# Approximate Multiplication and Squaring Circuits with Parallel Correction

Patricio Bulić[1], Jason Newman[2]

[1]Faculty of Computer and Information Science
University of Ljubljana

[2]Faculty of Electrical Engineering
University of Suburbia

# Agenda



- Motivation
- Approximate Multiplier and Squarer
- Hardware Implementation
- Error Analysis
- Conclusions

# Introduction



- Implementation bla bla:
  - bla bla bla
  - higher performance at smaller power consumption

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- Some beautiful chips:
  - noise and learning ability of analogue and digital designs
  - ASIC and FPGA (field programmable gate array)

# Introduction



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  - bla bla bla
  - higher performance at smaller power consumption
- Some beautiful chips:
  - noise and learning ability of analogue and digital designs
  - ASIC and FPGA (field programmable gate array)
- Signal processing applications incorporate complex algorithms with many multiplications
  - Multiplication is area, power and time consuming operation
  - bla bla bla

# Approximate Multiplier



- An approximate multiplier, introduced by Babic et al. (2010):
  - Reduced usage of logic resources: one adder and a shifter
  - Reduced power consumption
- The product of the two numbers, $N_1$ and $N_2$

$$N_1 \cdot N_2 \quad = \quad (2^{k_1} + N_1^{(1)}) \cdot (2^{k_2} + N_2^{(1)})$$

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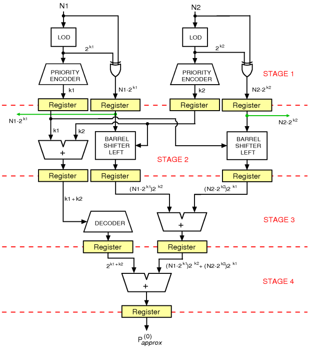
# Hardware Implementation



- A Basic block implements the approximate product

$$(N_1 \cdot N_2)_{approx} =$$



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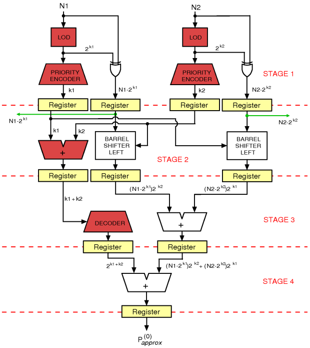

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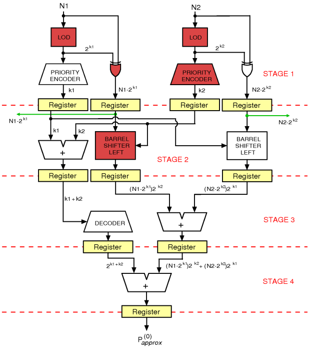

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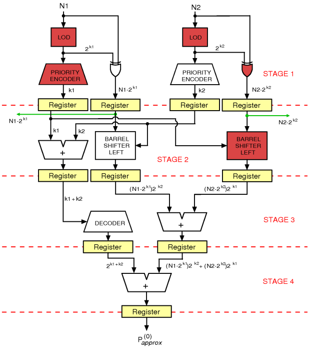

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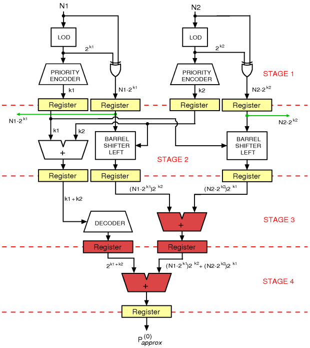


# Error Analysis



### Theorem

*The probability of an error in the circuit is directly proportional to the trouble it can cause.*

# Error Analysis



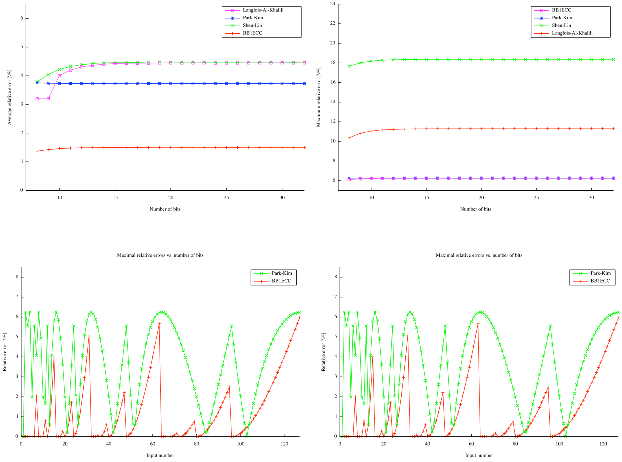
**Theorem**

*The probability of an error in the circuit is directly proportional to the trouble it can cause.*

**Proof.**

The proof is straightforward. □

# Errors

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# Conclusions



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- Error analysis has shown that an error in the circuit is directly proportional to the trouble it can cause.
- We can calculate the correction terms in parallel.