COMPUTER ARCHITECTURE

8 Memory Types & Technologies

8 Memory types & technologies - objectives:

- Basic understanding of:
  - The speed and access types
    - address based, associative
  - Static, Dynamic RAM
  - Synchronous Dynamic RAM (SDRAM)
- Understanding memory technologies:
  - Synchronous (pipeline) operation mode (SDRAM)
  - Flash memories
  - SSD, HDD drives

8 Memory types & technologies

Memory types & technologies in every-day use:

Technology	Type	Access
SRAM	Registers	Direct reg. addressing in instr. …
SRAM	Caches	(transparent operation)
SDRAM, Flash	Main memories (DDRx, NOR flash)	Direct with memory access instr. (e.g. LDR, STR)
flash (USB,SSD), magn. tapes, discs (HDD), optical disks	Secondary memories USB,SSD (NAND flash),HDD, CD, …	Indirect via I/O controllers

Types of memories:

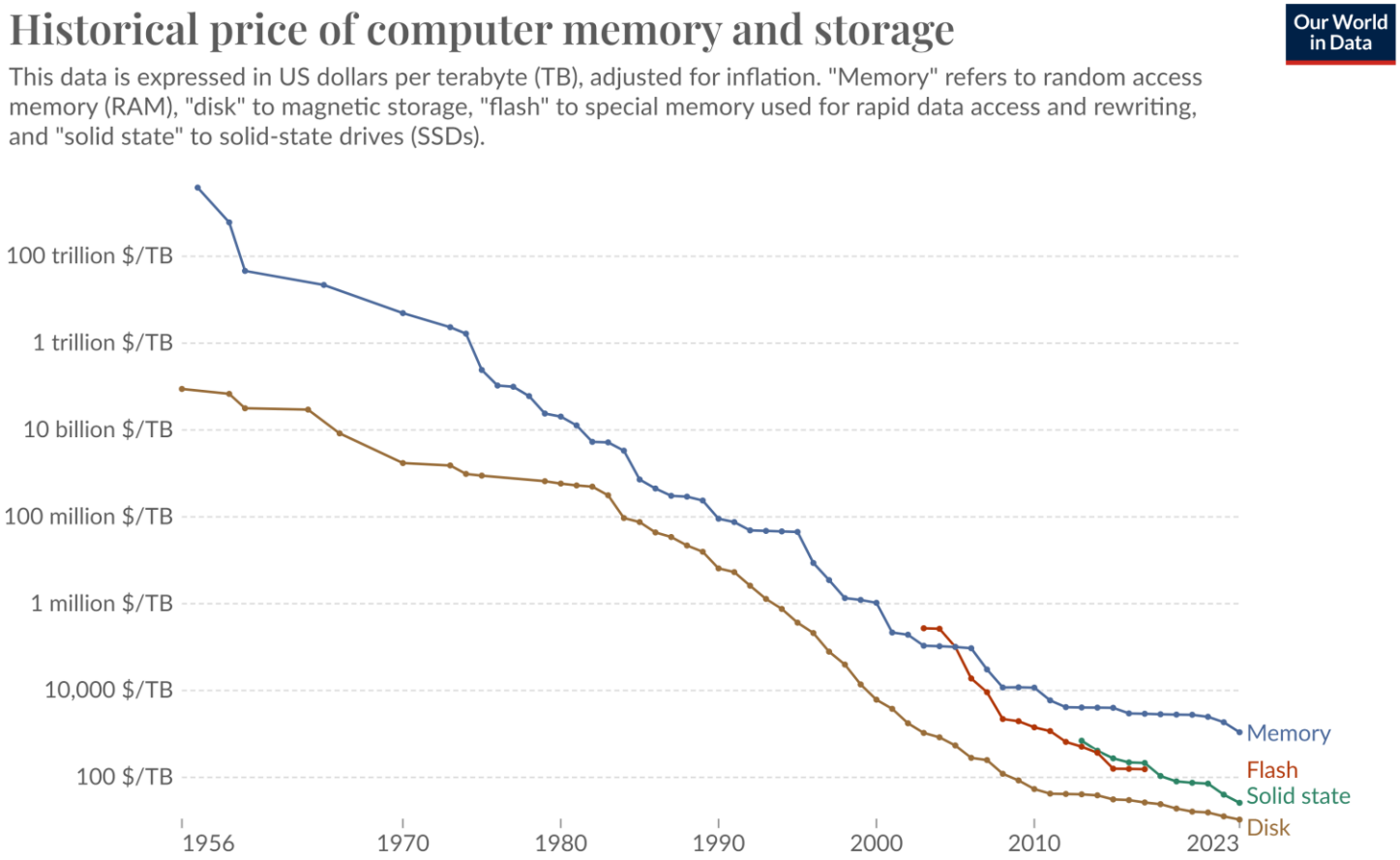
- Main memory (also primary memory)
- Auxiliary memory (also secondary memory, mass memory) - considered also as the I/O device.
- The difference between the main memory and auxiliary memories:
  - CPU has **direct access** to the main memory using machine instructions (eg. the LOAD, STORE).
  - Access to the auxiliary memory (SSD, HDD, tapes, CDs and DVDs) is **indirect** via I/O commands in I/O program.

- Reasons for primary-secondary division:
  - long time ago technological (with existing technology we could not produce the main memory greater than a few thousand words)
  - Today reasons are more economic

Memory Type	Price for 1 GB (dec. 2017)
Main memory - SDRAM (DDR3, DDR4)	<10 € / GB
Auxiliary memory - SSD (solid state drive)	<0,5 € / GB
Auxiliary memory - HDD (magnetic disk)	<0,05 € / GB

SDRAM - Synchronous Dynamic Random Access Memory - Synchronous Dynamic RAM
SSD - Solid State Drive - Solid State Drive
HDD - Hard disk Drive - Hard (magnetic) disk

Price [USD/MB]



LOG

https://ourworldindata.org/grapher/historical-cost-of-computer-memory-and-storage

8.1 Properties of memories

- Properties of the memories can be evaluated in respect to a variety of criteria:
  - Price - *[€ / GB]*
  - Speed: access time - t_a *[ns]* and access speed b_a *[B/s; B/s, T/s]*
  - Access mode - addres/content
  - Variability of content – read-only (ROM) / read-write (RAM)
  - Persistence of content - volatile/non-volatile
  - Reliability - the probability of the occurrence of errors

The time and speed of access

- The memory capacity is determined by the speed of reading and writing of information in memory.
- As a measure of the speed is commonly used the average time it takes to read a word from memory.
- This time is called **access time** (access time) and labeled with t_a and measured in [ns].

- **Access time t_a** is commonly defined as the time that elapses from the moment when the memory address is obtained by the memory, until the moment:
  - In case of **reading:** the requested information is presented at the output of the memory
  - In case of **writing:** information at the input of the memory is no longer needed
- Time to write is in most of today's memories about the same time as for reading.

- **Access rate b_a** determines the maximum number of transferred words or bits or bytes per second, or even transfers per second.

- In DRAM memories, certain additional time is needed after each access (denoted as dead time t_m) before the next access begins (other influencing factors).

- In the DRAM memories, access speed b_a is therefore defined as:

$$b_a = \frac{1}{t_a + t_m} = \frac{1}{t_c}$$

Units: b/s - bits/second or
B/s - bytes/second or
T/s - transfers/second

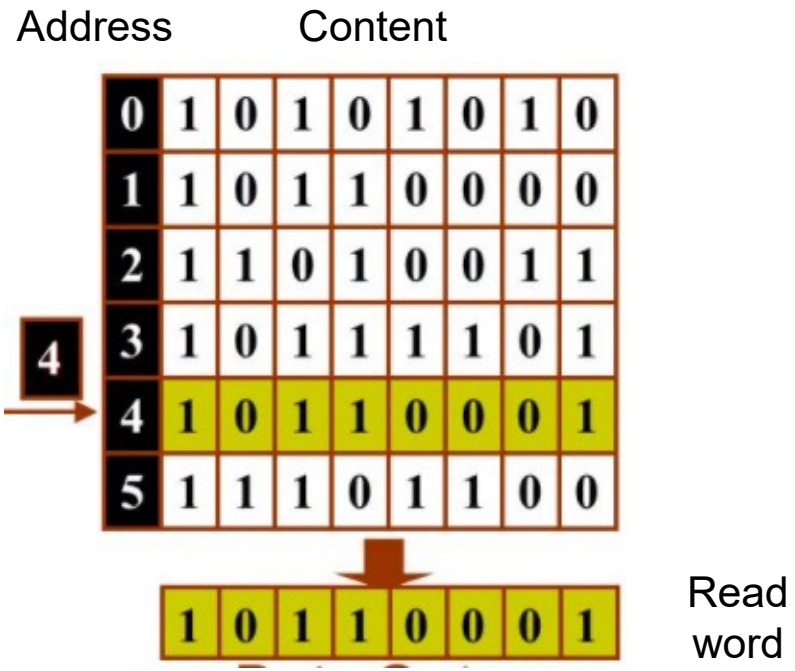
- Time t_c represents the cycle time – the time between two successive accesses.

Access Modes

- According to the selection method for memory to which we want to access, the memories are divided into two groups:
  - **A. Conventional memories** - each memory location (word) has a fixed address, access to the selected word is via address
  - **B. Associative memory** - memory words have no address, access to the desired word is via the content or part of the content of this word
    - Associative memories are also known as „content-addressable“.

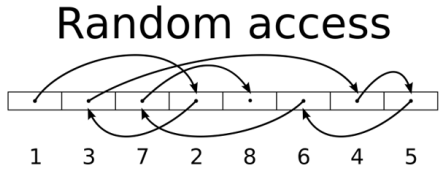
A. Conventional memories:

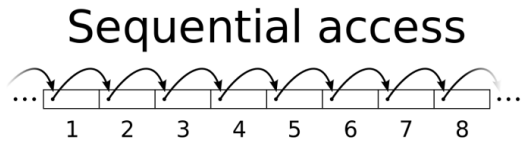
- access to the selected word is via address

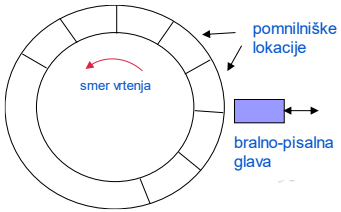


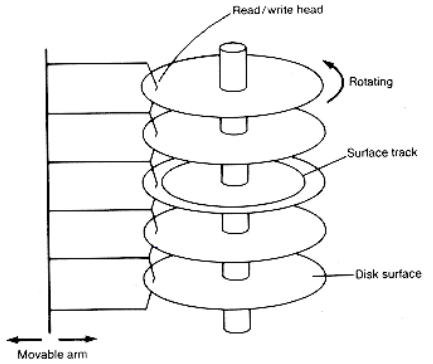
A. Conventional memories - access by address of mem. location

- Among conventional (address-based) memories, we have with different types of memories, four different access modes:
  - random access (semiconductor - solid state memories)
  - sequential access (e.g. magnetic tapes)
  - circular access (e.g. magnetic drums)
  - direct access (magnetic disks, optical disks)

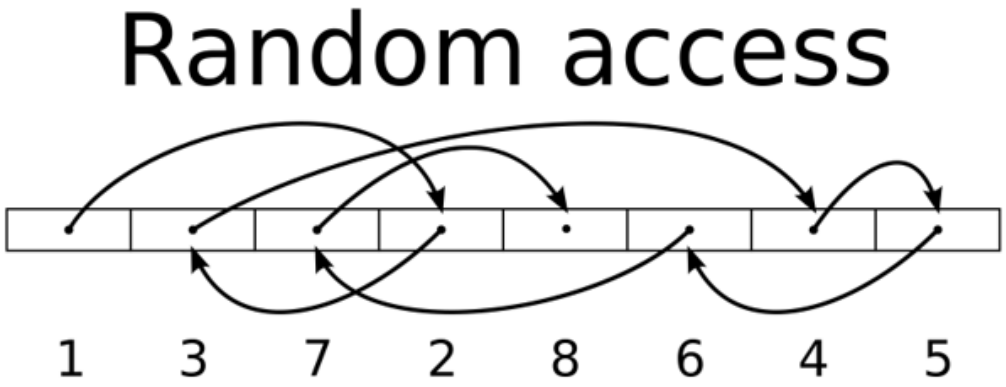




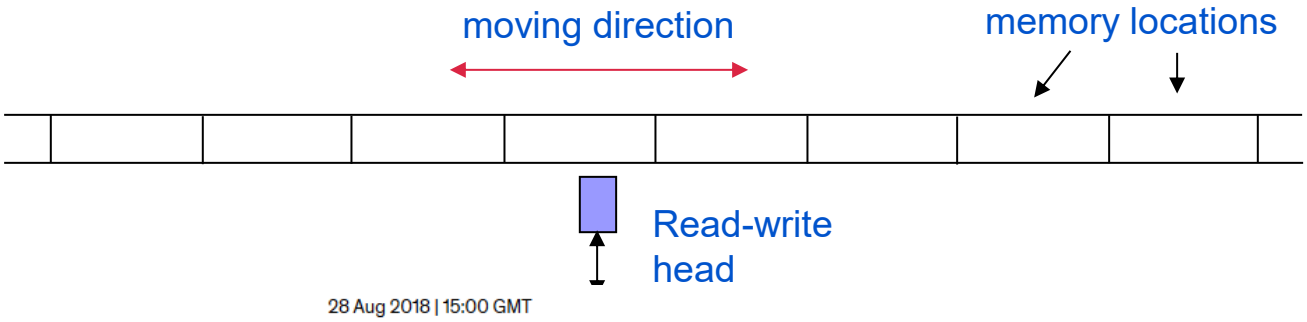


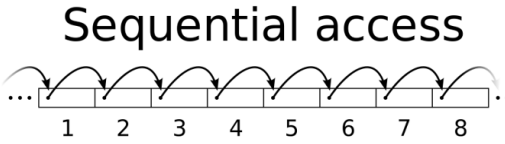


- **Random access (random access)**
  - Access time to any memory word (location) is independent of the address and the sequence of all previously addressed words.
  - Each memory location can be accessed through the addressing logic circuit in the same time t_a, irrespective of the previously addressed location.
  - All semiconductor memories (solid-state memory) are random access memories.



- **Serial access (sequential access)**
  - Access time depends on the address of previously accessed word.
  - This means that the access time t_a strongly depends on the sequence of addresses to which we want to access
  - Magnetic tape is an auxiliary memory with sequential access





28 Aug 2018 | 15:00 GMT

Why the Future of Data Storage is (Still) Magnetic Tape

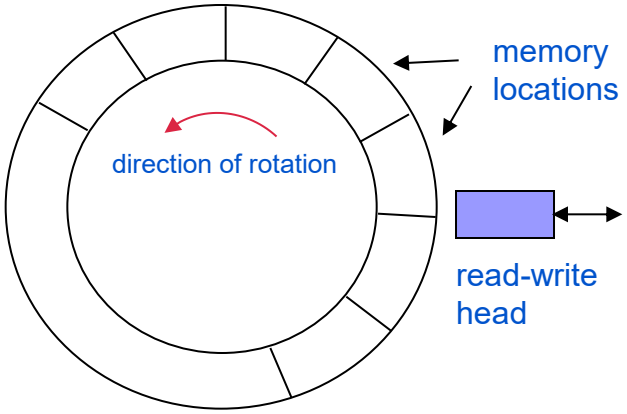
Disk drives are reaching their limits, but magnetic tape just gets better and better

IBM Makes Tape Storage Better Than Ever ›IBM just shattered previous records for magnetic tape's data storage capabilities, ensuring it meets demand for the next decade

BY DEXTER JOHNSON | 17 DEC 2020 | 3 MIN READ

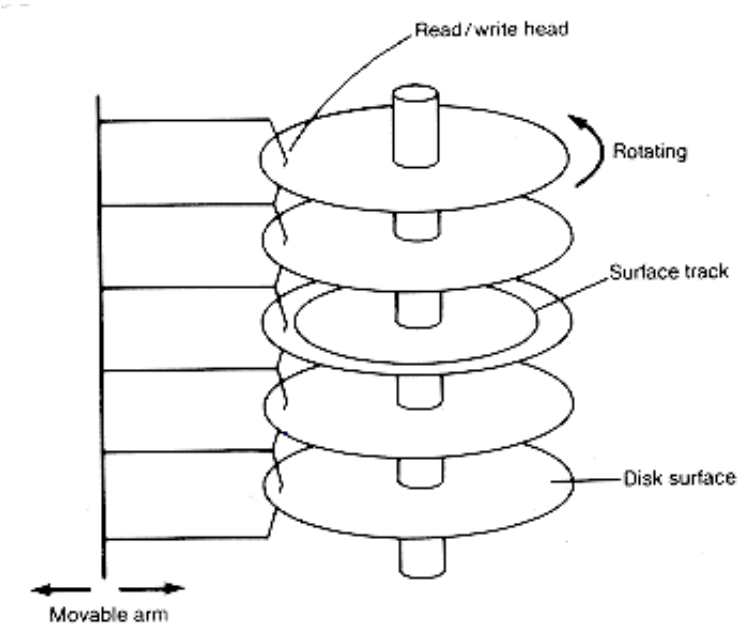
Rotational access (circular access)

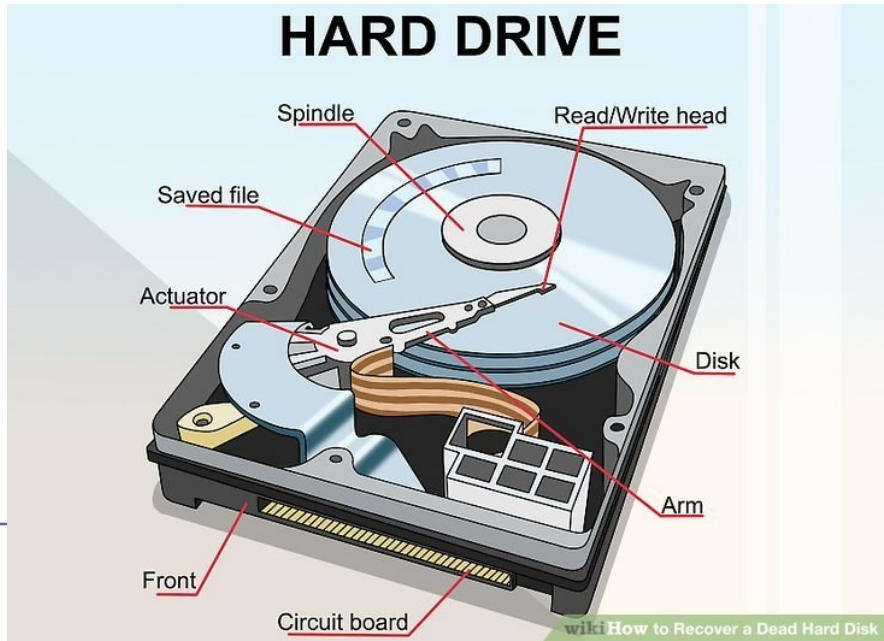
- A special type of sequential access, where the memory locations are arranged in a circle.
- Average access time t_a is half the time of one revolution.
- Examples of memories with a rotational access are magnetic drum and the magnetic disk with a fixed read-write heads.



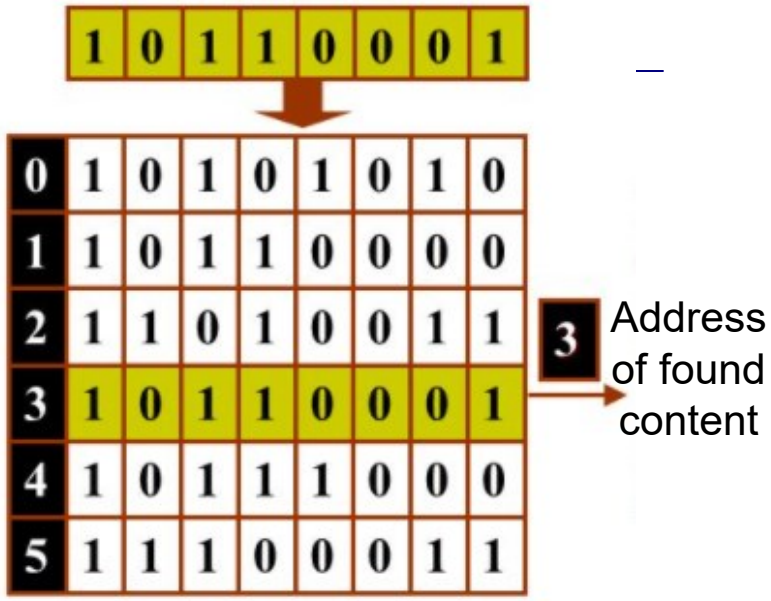
Direct access

- Is a combination of sequential and rotational access, which is used in magnetic and optical disks with movable heads.
- Recordings on the magnetic disk are in the form of concentric circles (tracks), memory locations (sectors) are arranged along the tracks.
- Read write head is first moved to the appropriate track (sequential access) and then the circular access is used to a desired location on the track.

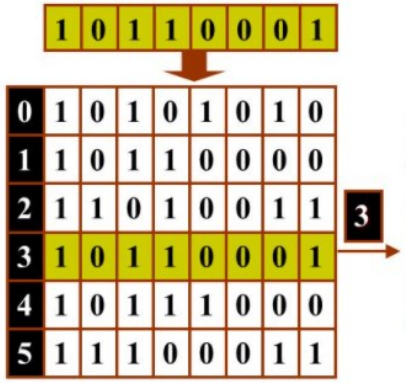




B. Associative memory - access via the content of mem. location



- Associative memory - memory locations don‘t have addresses.
- Access to the certain memory word is via the content (or part of the content).
- Finding content is realized electronically with additional logic ci all words simultaneously (in parallel).
- Realization requires a complex logic circuit, therefore associati memories are rarely bigger than a few 100 words.



- Associative memory
  = content-addressable
  = parallel-searchable

- Access time t_a is due to the comparison of the content slightly longer than the address-based memories.

- Search for specific content in the associative memory is very fast $\Rightarrow$ applicable in caches

- Search for specific content in conventional memory lasts much longer.

- Associative memory – Example use in routers:

TABLE I
EXAMPLE ROUTING TABLE

Entry No.	Address (Binary)	Output Port
1	101XX	*A*
2	0110X	*B*
3	011XX	*C*
4	10011	*D*

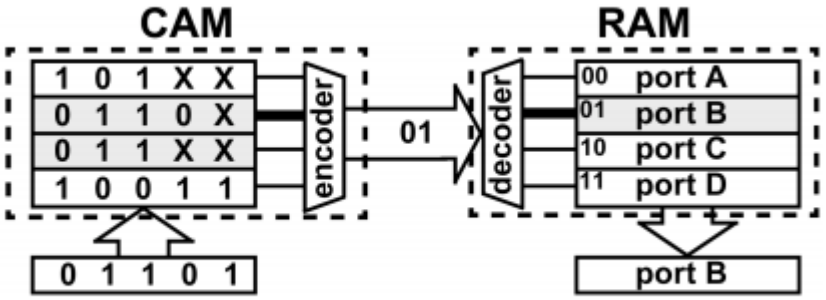


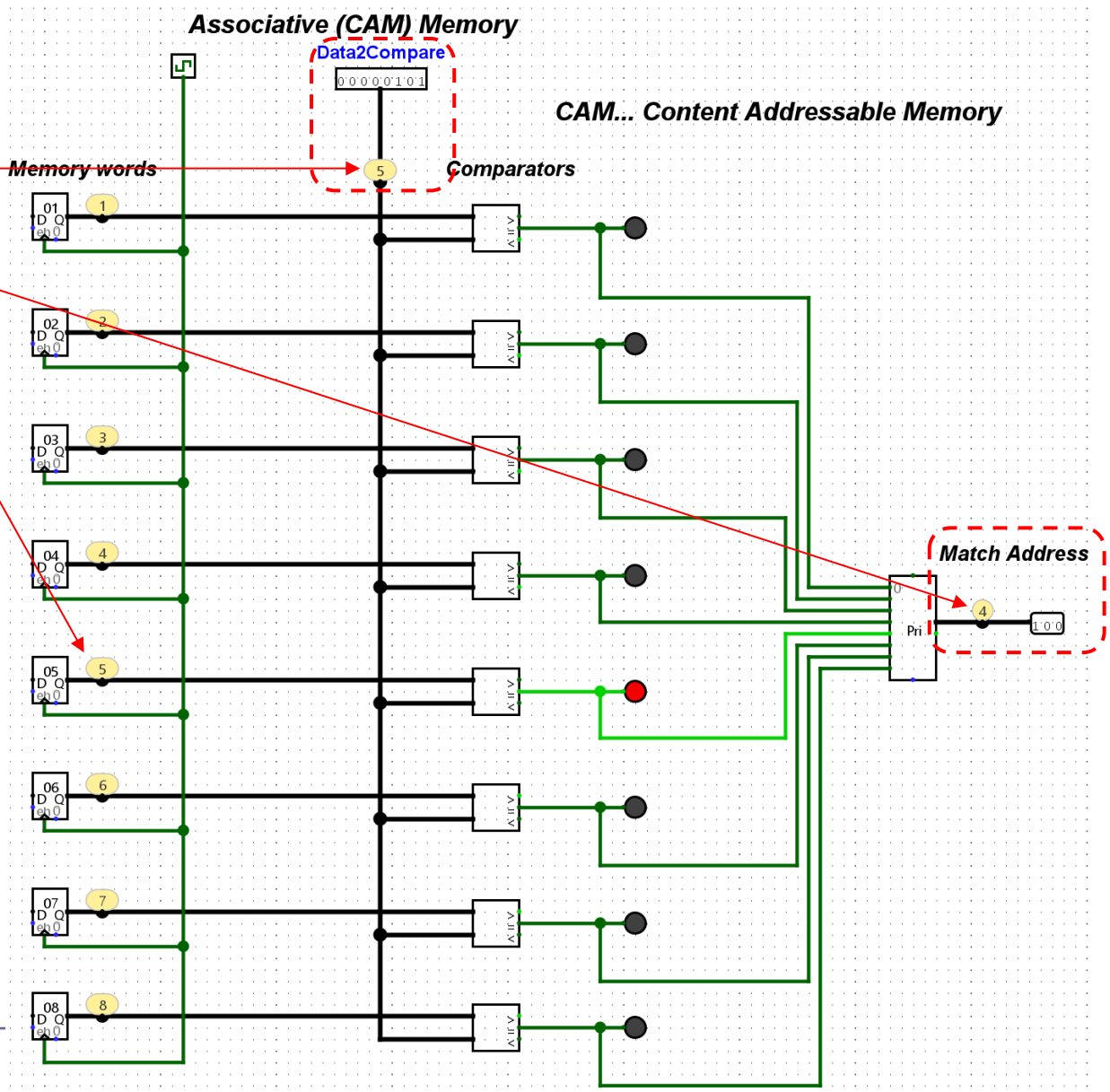
Fig. 3. CAM-based implementation of the routing table of Table I.

712 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 41, NO. 3, MARCH 2006

Content-Addressable Memory (CAM) Circuits and Architectures: A Tutorial and Survey

Kostas Pagiamtzis, *Student Member, IEEE,* and Ali Sheikholeslami, *Senior Member, IEEE*

- Associative memory
- Example in Logisim:
  - Where is value 5 ?
    - Ans.: On address 4



8.2 Memory Technologies

- Today, for production of memories we use three basic technologies:
- Semiconductor (solid-state) Memories:
  - ROM Read only Memory
    - PROM, EPROM, EEPROM
  - RAM (Random Access Memory)
    - SRAM (Static RAM), DRAM (Dynamic RAM)
  - Flash Memories (special type of EEPROMs)
- Magnetic storage devices (magnetic disks, magnetic tapes)
- Optical storage devices (CD, DVD, BD - Blu-ray)

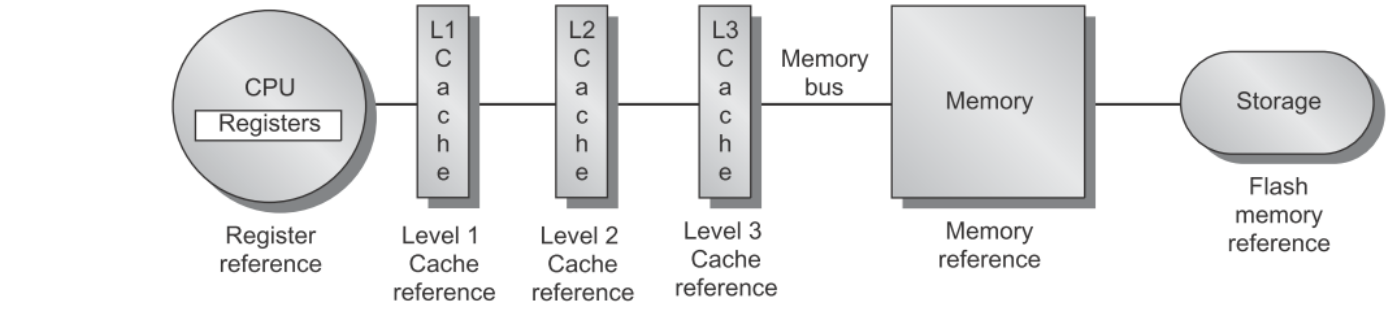
Memory technologies - overview

	access time	Price for 1GB (dec. 2015)	Application
SRAM (semiconductor memory)	0,5 – 2,5 ns	200 – 700 €/GB	Caches, registers
SDRAM (semiconductor memory)	35 – 50 ns	< 6 €/GB	main memory
SSD (solid-state memory)	$5*10^3$ – $200*10^3$ ns = 5 µs – 200 µs	< 1 €/GB	virtual memory permanent memory
HDD (magnetic memory)	$3*10^6$ – $15*10^6$ ns = 3 ms – 15 ms	< 0,1 €/GB	virtual memory permanent memory

Magnetic disk ≈ 10,000,000 - times slower than a static SRAM memory

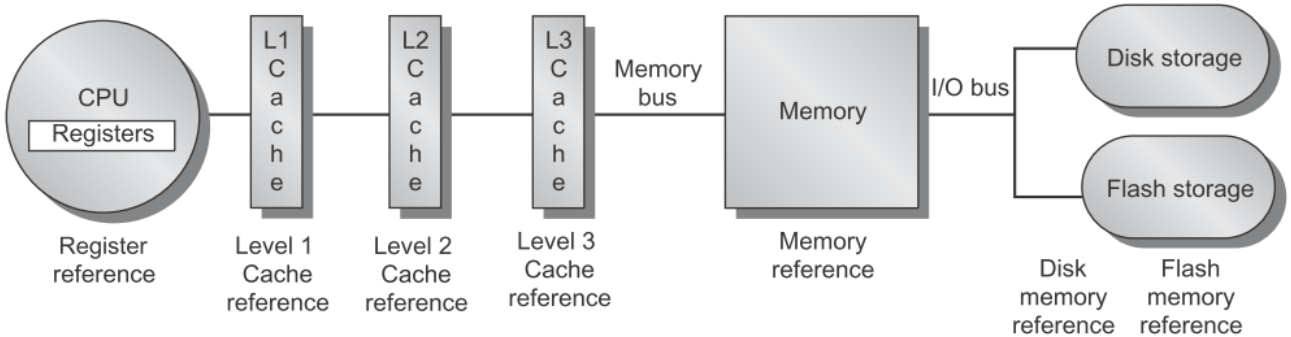
SRAM - Static RAM (Static Random Access Memory)
SDRAM - Synchronous Dynamic RAM
SSD - Solid State (flash) Disk (Solid State Drive)
HDD - Hard disk Drive

Memory technologies in memory hierarchy [Patt]



Laptop	Size:	1000 bytes	64 KB	256 KB	4-8 MB	4–16 GB	256 GB-1 TB
	Speed:	300 ps	1 ns	3–10 ns	10–20 ns	50–100 ns	50-100 uS
Desktop	Size:	2000 bytes	64 KB	256 KB	8-32 MB	8–64 GB	256 GB-2 TB
	Speed:	300 ps	1 ns	3–10 ns	10–20 ns	50–100 ns	50-100 uS

(B) Memory hierarchy for a laptop or a desktop



Size:	4000 bytes	64 KB	256 KB	16-64 MB	32–256 GB	16–64 TB	1-16 TB
Speed:	200 ps	1 ns	3–10 ns	10–20 ns	50–100 ns	5–10 ms	100-200 us

(C) Memory hierarchy for server

- Semiconductor memories (ROM, SRAM, DRAM and partially Flash Memories) are random access memories (Random Access).
  - Minimum memory unit is one-bit memory cell.
  - Minimum addressable memory location is a memory word.
  - Each memory location can be accessed via logic circuits for addressing in the same time irrespective of the previously addressed location.
  - Access time is always the same, irrespective of the address and the sequence of addresses currently used.

Semiconductor memories comparison

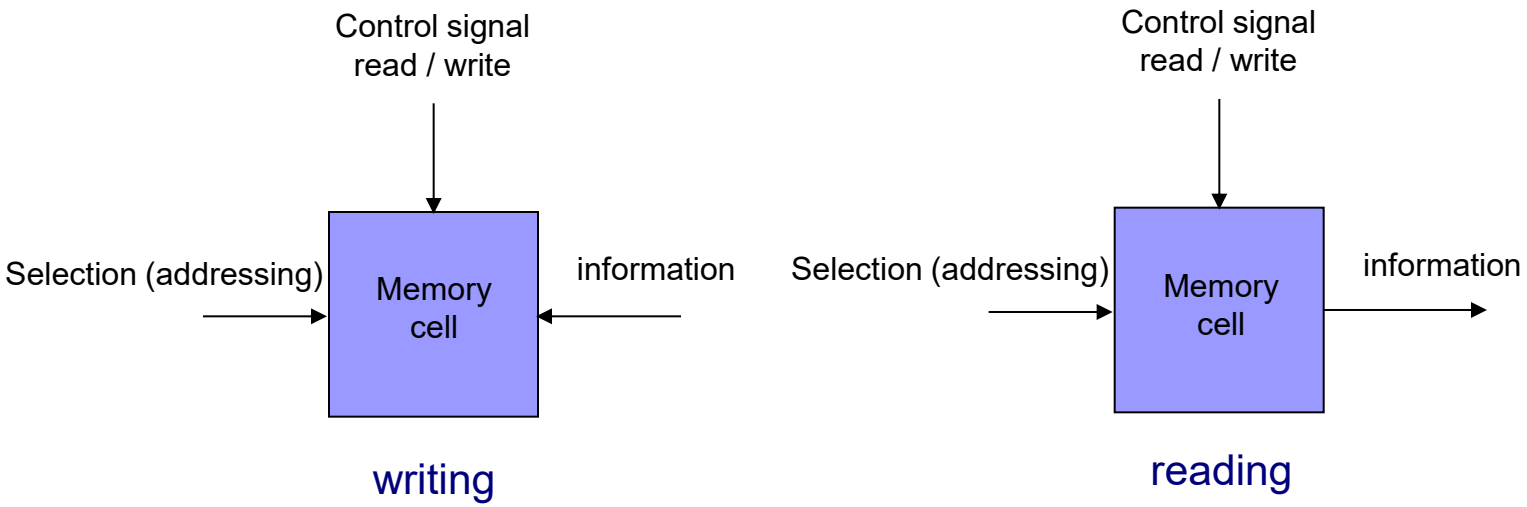
Type of semiconductor memory	Access Mode	Access Type	Deleting content	Write method	Persistence content after switching off the power supply
RAM	random	Read-write memory	Electrically - each byte	electrical	volatile
ROM	random	Read-only memory	Not possible	The mask in production	non-volatile
PROM				Electrically in programming device	
EPROM	random	Mostly read memory	UV light - the whole chip		
EEPROM			electrically - each byte	electrical	
NAND Flash	Random on level of page	Read-write memory	electrically - each block		

RAM - Random Access Memory
ROM - Read only Memory
PROM - Programmable ROM
EPROM - Erasable PROM
EEPROM - Electrically Erasable PROM

- One-bit memory cell is realized by the transistors

  (Transistor = semiconductor element -> therefore the name „semiconductor memories“)

  - Memory cell can be in one of two possible stable states, representing a value of 0 or 1,
  - it is possible to write (at least once), and set the state of 0 or 1,
  - State of the cell can be read or detected (sensed)

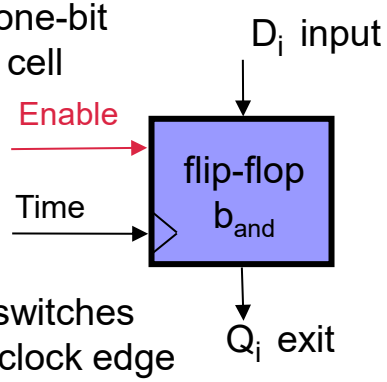


Flip-flop - one-bit memory cell

(one-bit register)

b_0

Flip-flop = one-bit memory cell

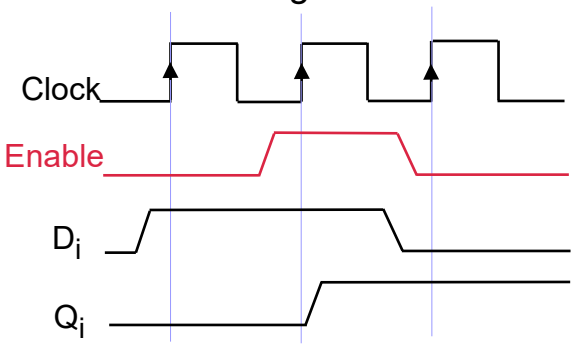


Flip-flop switches on positive clock edge

Truth Tables

Clock	En	D_i	Q_i
↑	0	0	Q
↑	0	1	Q
↑	1	0	0
↑	1	1	1

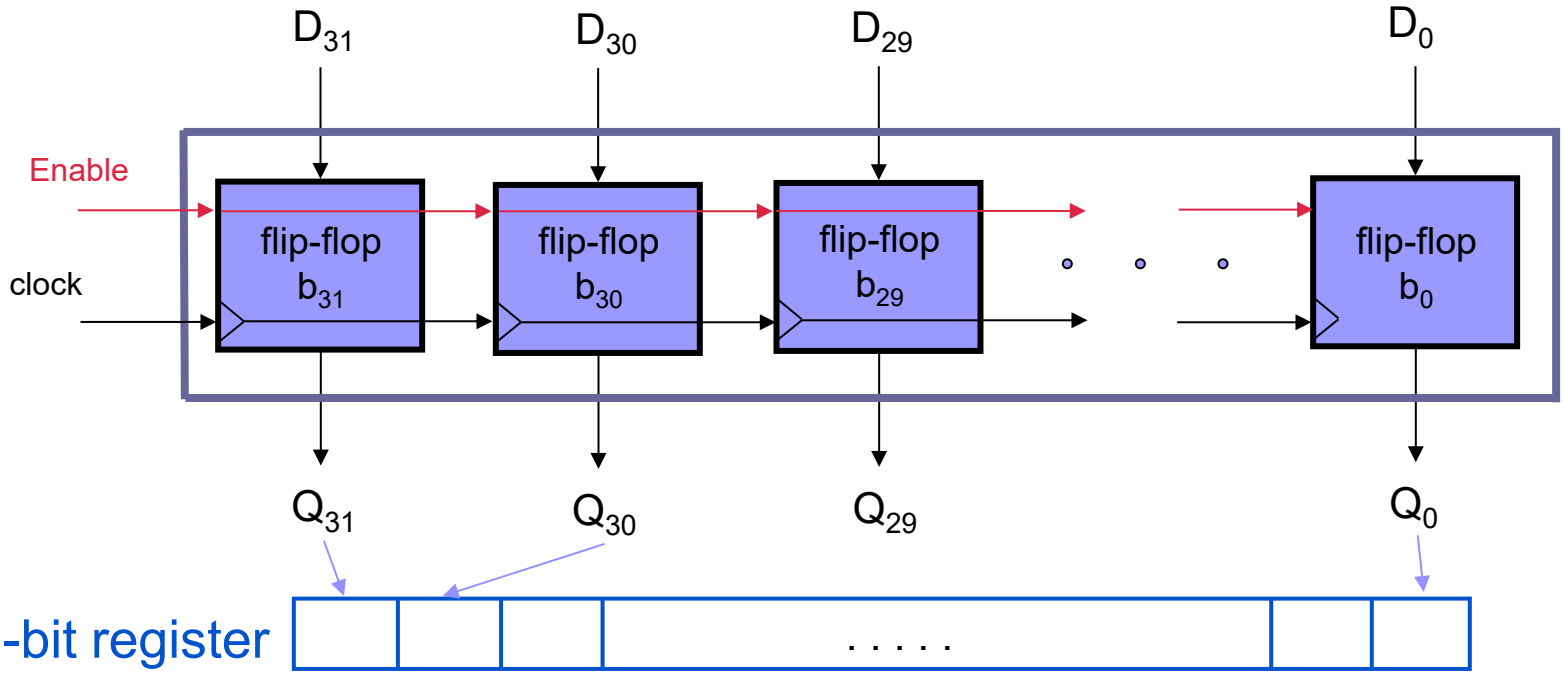
time diagram



The register as a sequence of memory cells

A 32-bit register

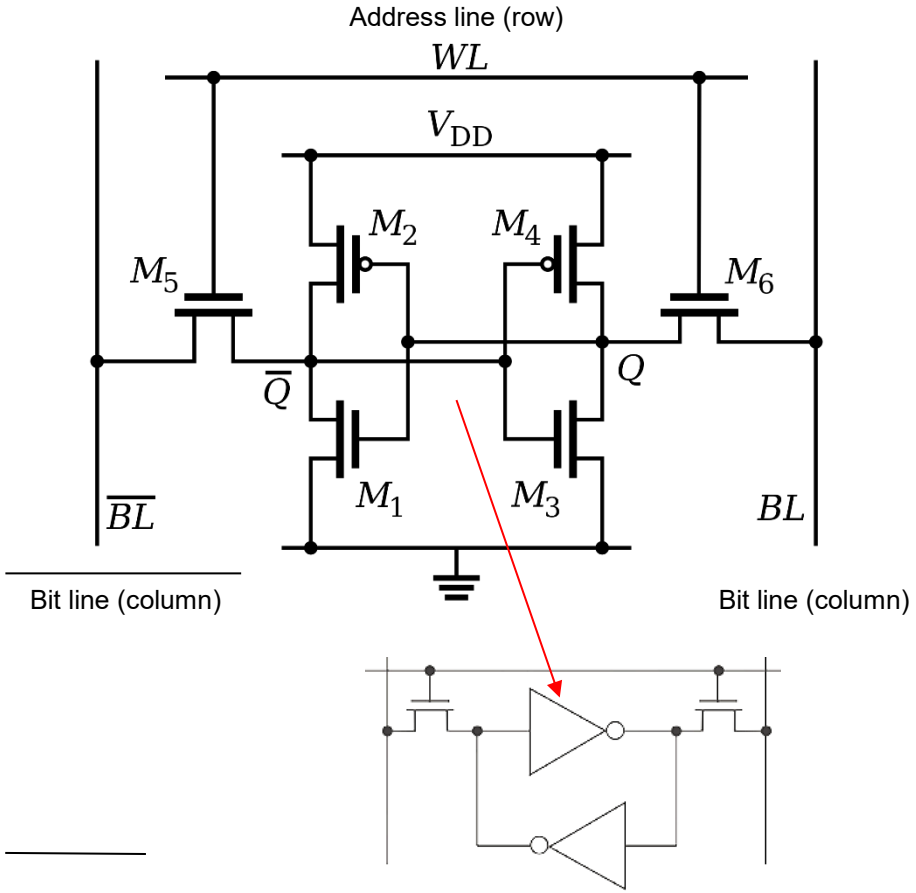
32 Flip-flops - 32 connected one-bit memory cells to operate in parallel



8.2.1 SRAM - static RAM

- **SRAM memory cell** is built as a flip-flop, typically with six transistors.
- Bit, which is written in the SRAM cell, remains unchanged until the new content is written in the cell.
- SRAM memory cell retains its contents only while it is connected to the power supply.
- Access time is short (0.5 to 2.5 ns), because the switching of transistors from one state to another is very fast.

SRAM (Static RAM) memory cell

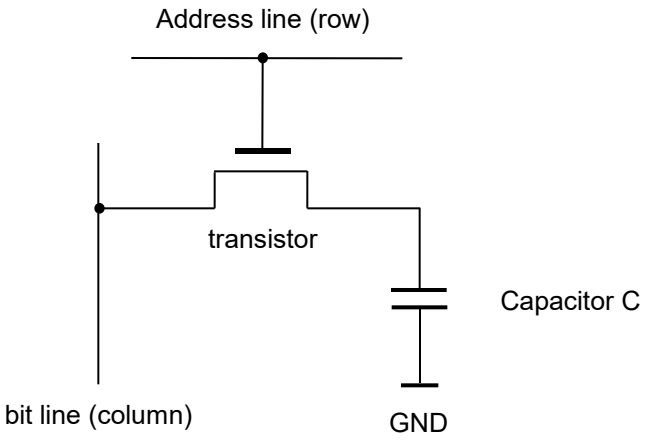


M_1 - M_6 transistors
V_{DD} supply voltage

8.2.2 DRAM - Dynamic RAM

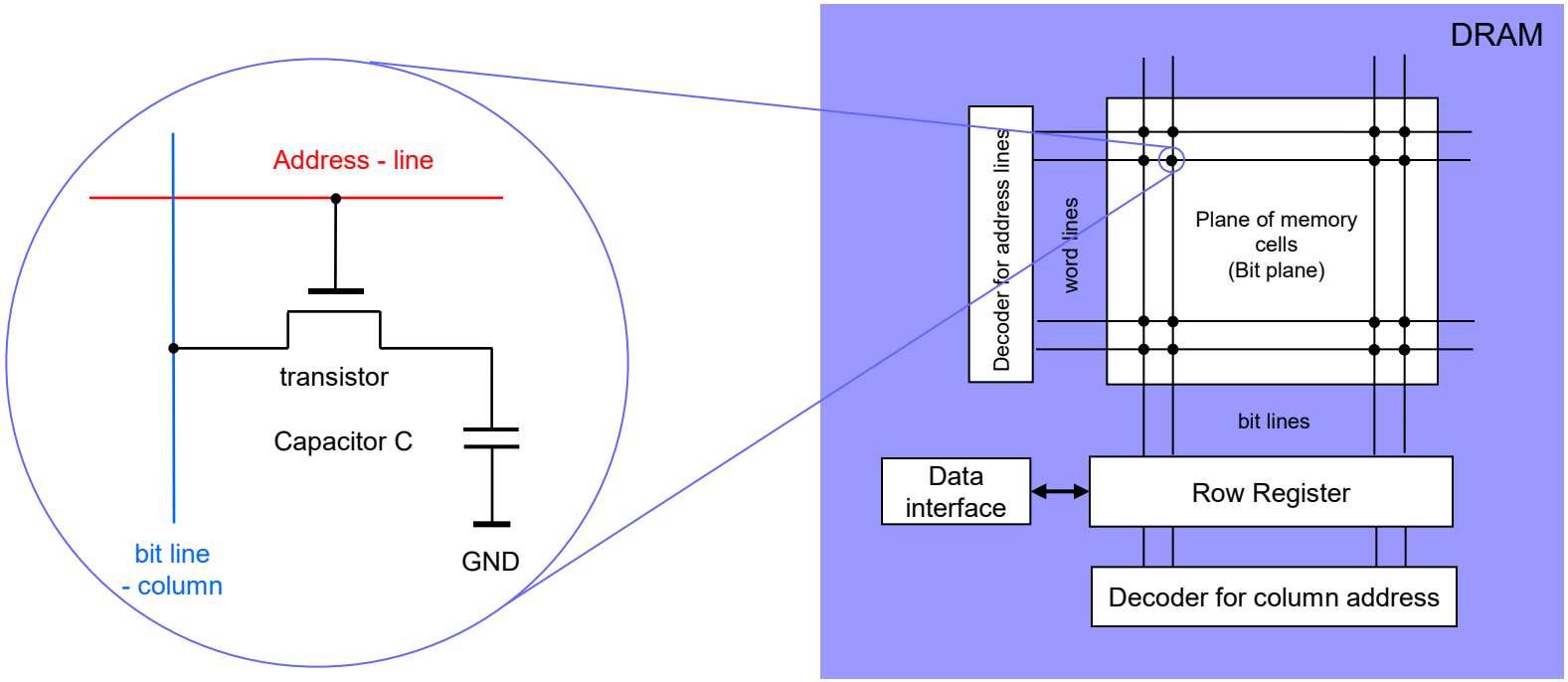
- **DRAM memory cell** is built with a transistor and a capacitor with a very small capacitance (C < 0.1 pF)
- Information, which is written in DRAM cell, is stored in the form of a charge on the capacitor.
- The charge on the capacitor is not permanent (T = few 10 ms), and thus, the contents of the DRAM memory cells has to be periodically renewed (refreshed).
- With today's technology, it is necessary to refresh the entire content of the memory chip every 64 ms (DDR2).

DRAM (Dynamic RAM) memory cell

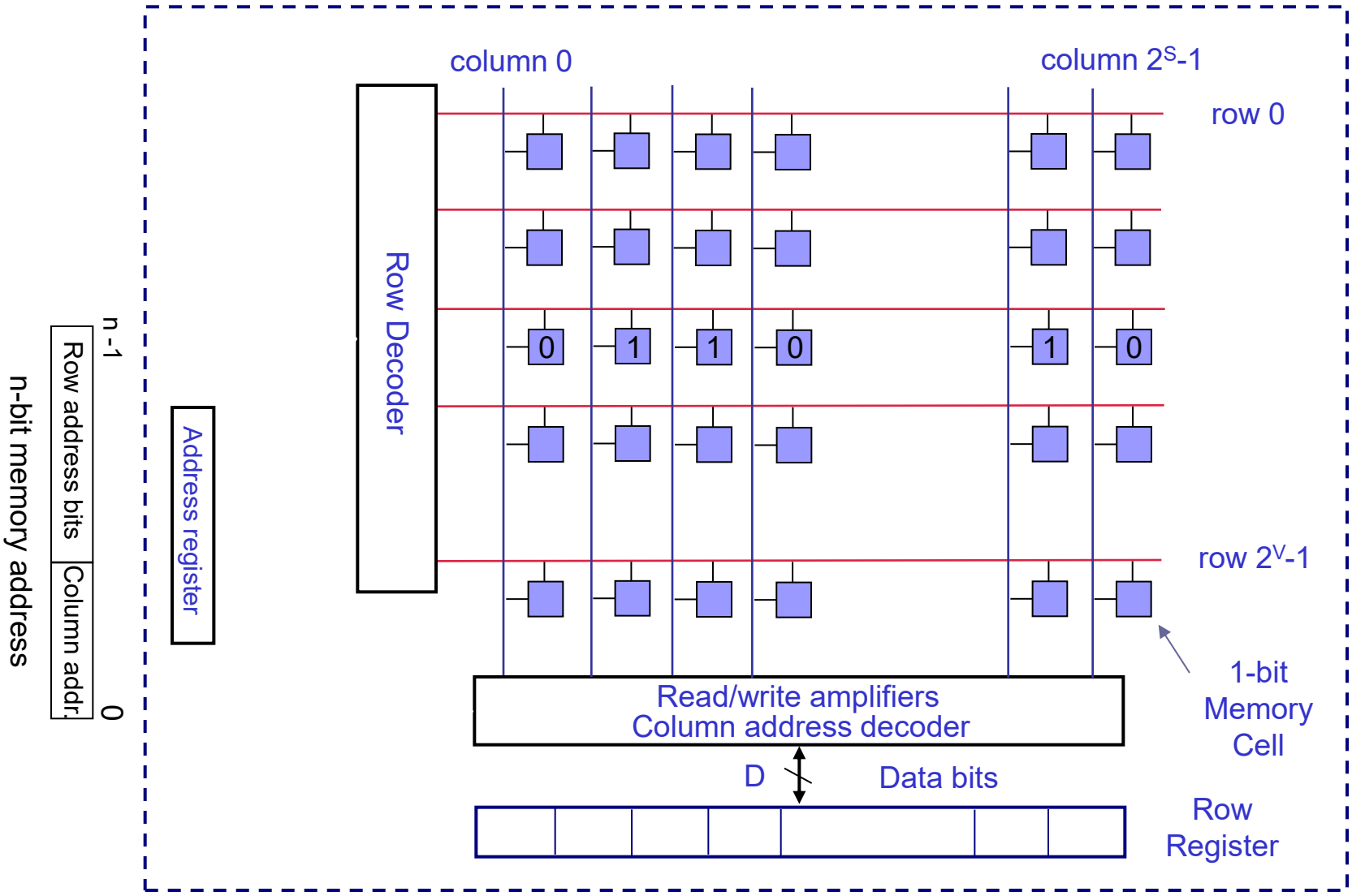


- The access time to the DRAM memory cell is 10 to 100 times longer than in the SRAM, because for changing from one state to another (0 → 1 or 1 → 0) it is necessary to charge or discharge the capacitor.
- Since the capacitance of the capacitor is very small (a few 10 fF, femtoFarad = 10^{-15} F) the charge on the capacitor is quickly lost and the stored information must be periodically refreshed (in today's technology, every 64 ms (milliseconds))
- Refresh cycles of the DRAM memory chips today represents typically 1 to 2% of the working time of DRAM memory.
- For reading and writing, therefore, 98 to 99% of cycles can be used.

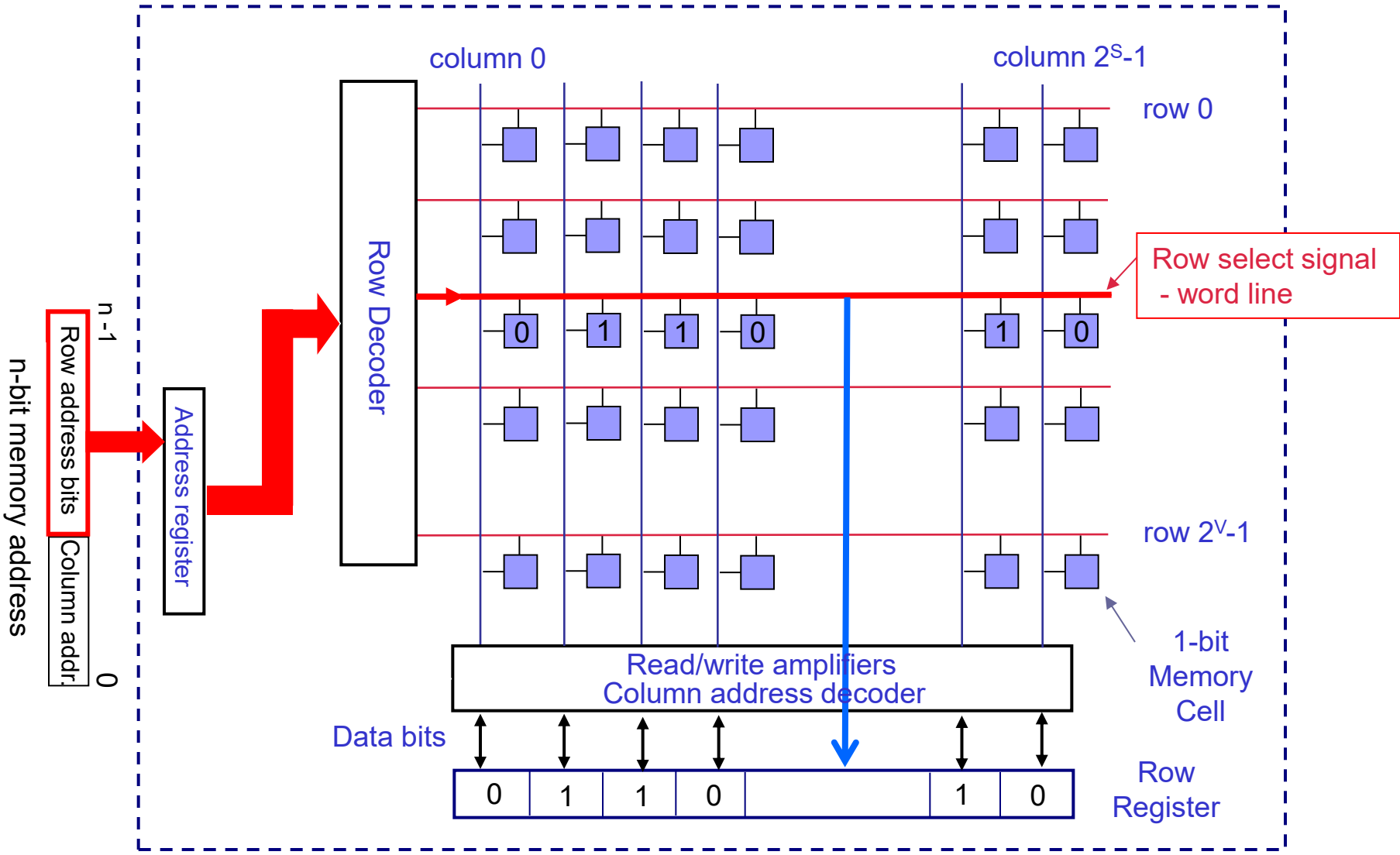
- one-bit DRAM memory cells are arranged in the form of a rectangular plane with rows and columns, called bit-plane.



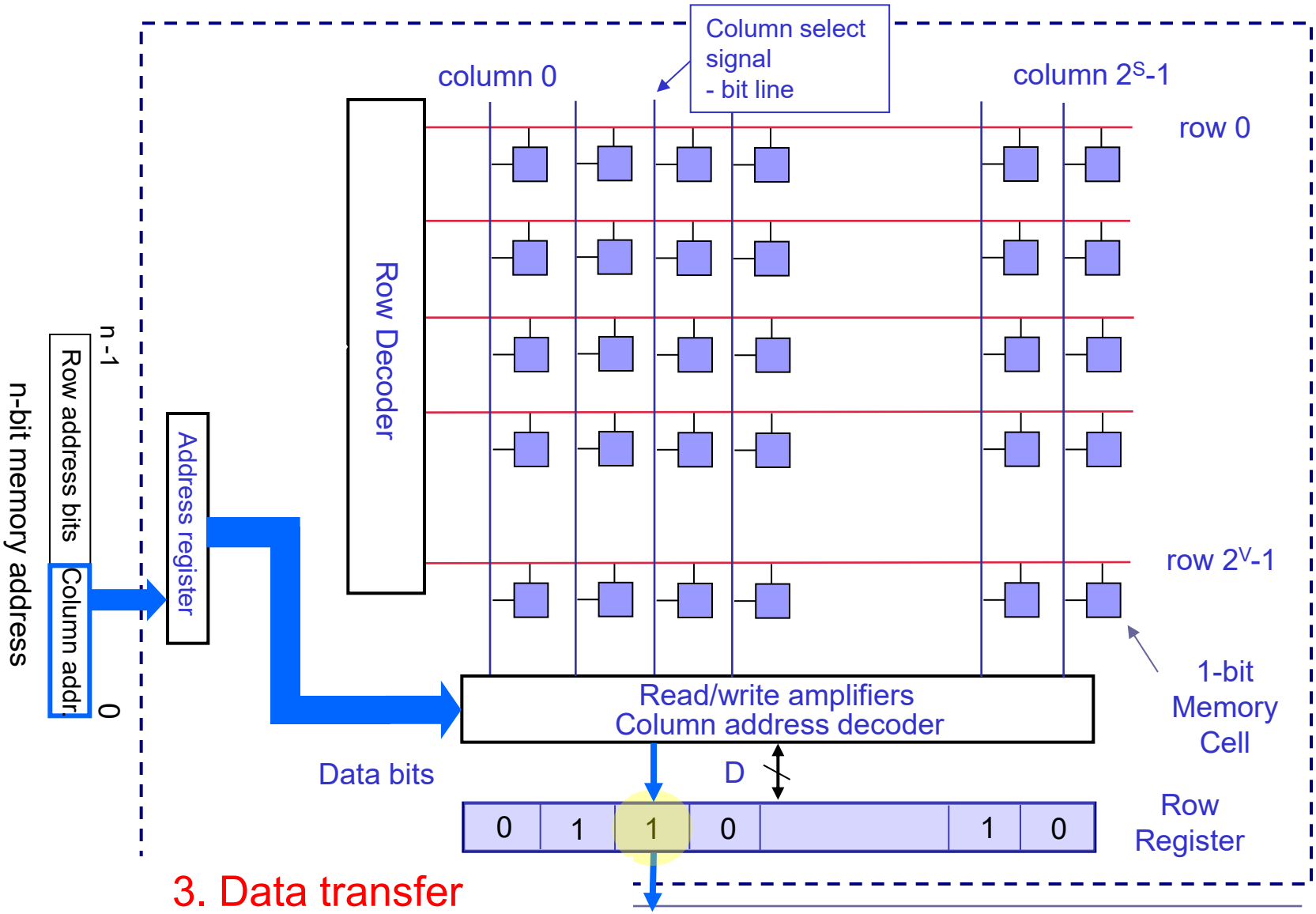
Bit plane organization



1. Read row into register

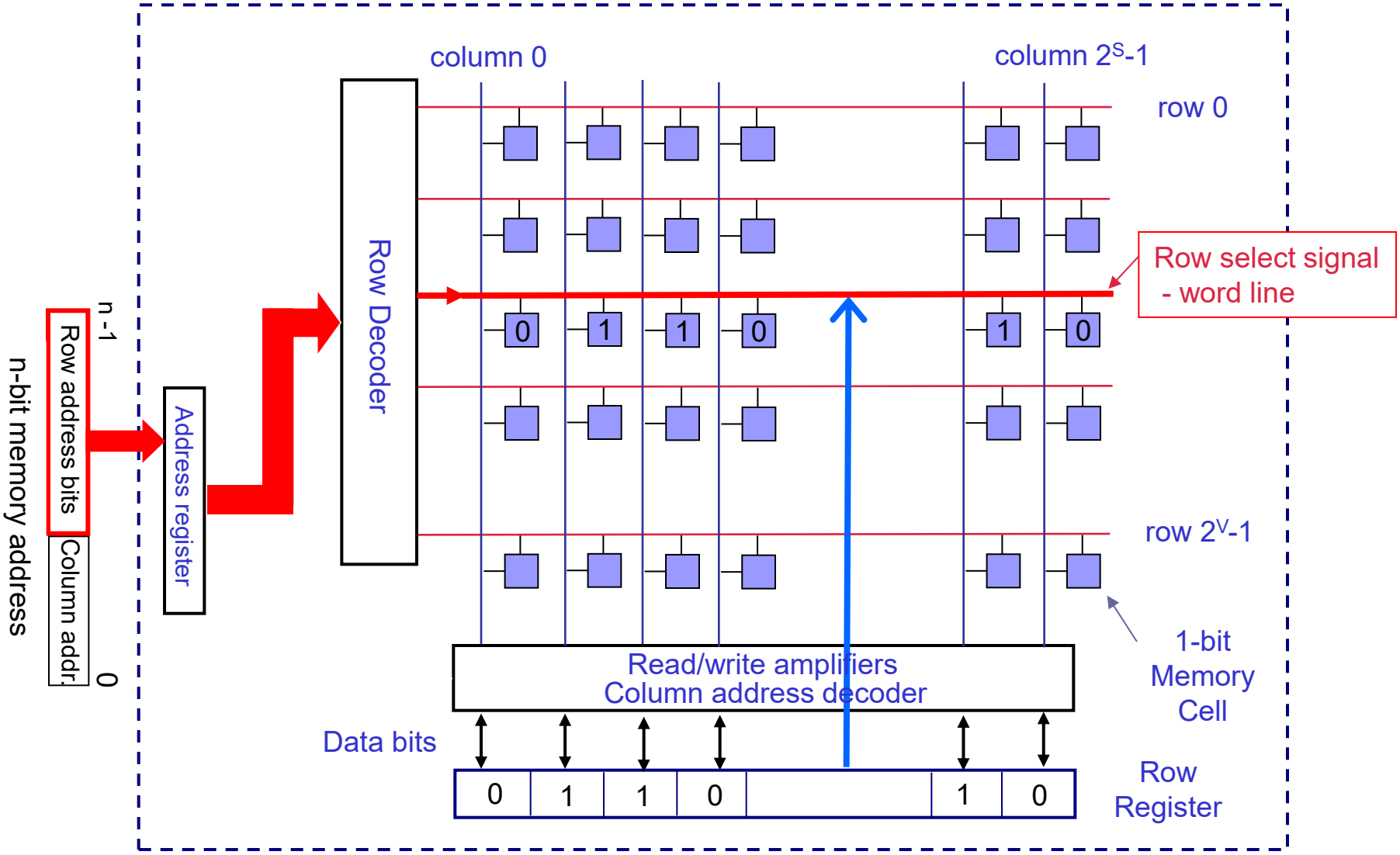


2. Bit selection (column address) from register

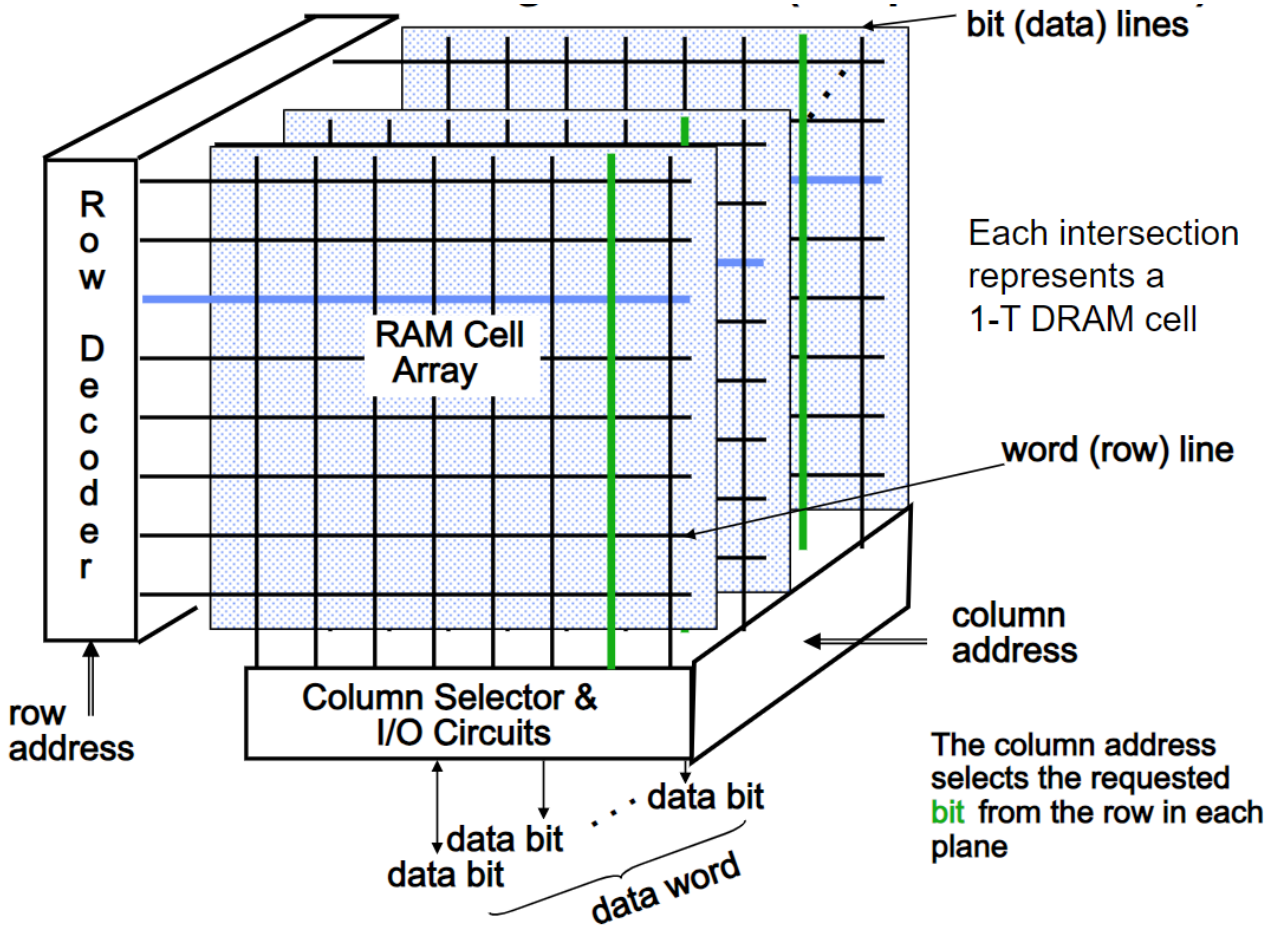


3. Data transfer

Write row back to row of cells- destructive read



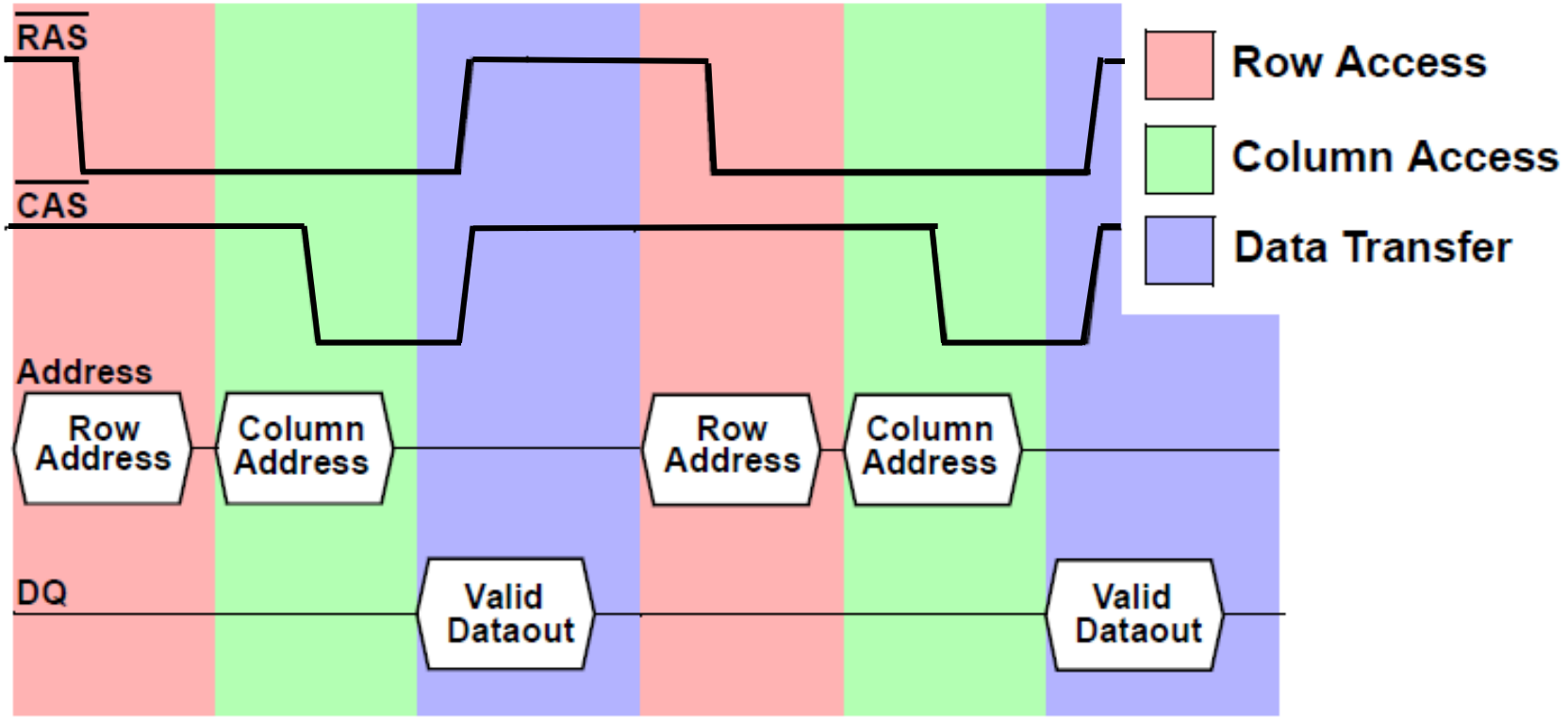
- Bit-planes are connected to form memory locations



Web: https://slideplayer.com/slide/10393094/

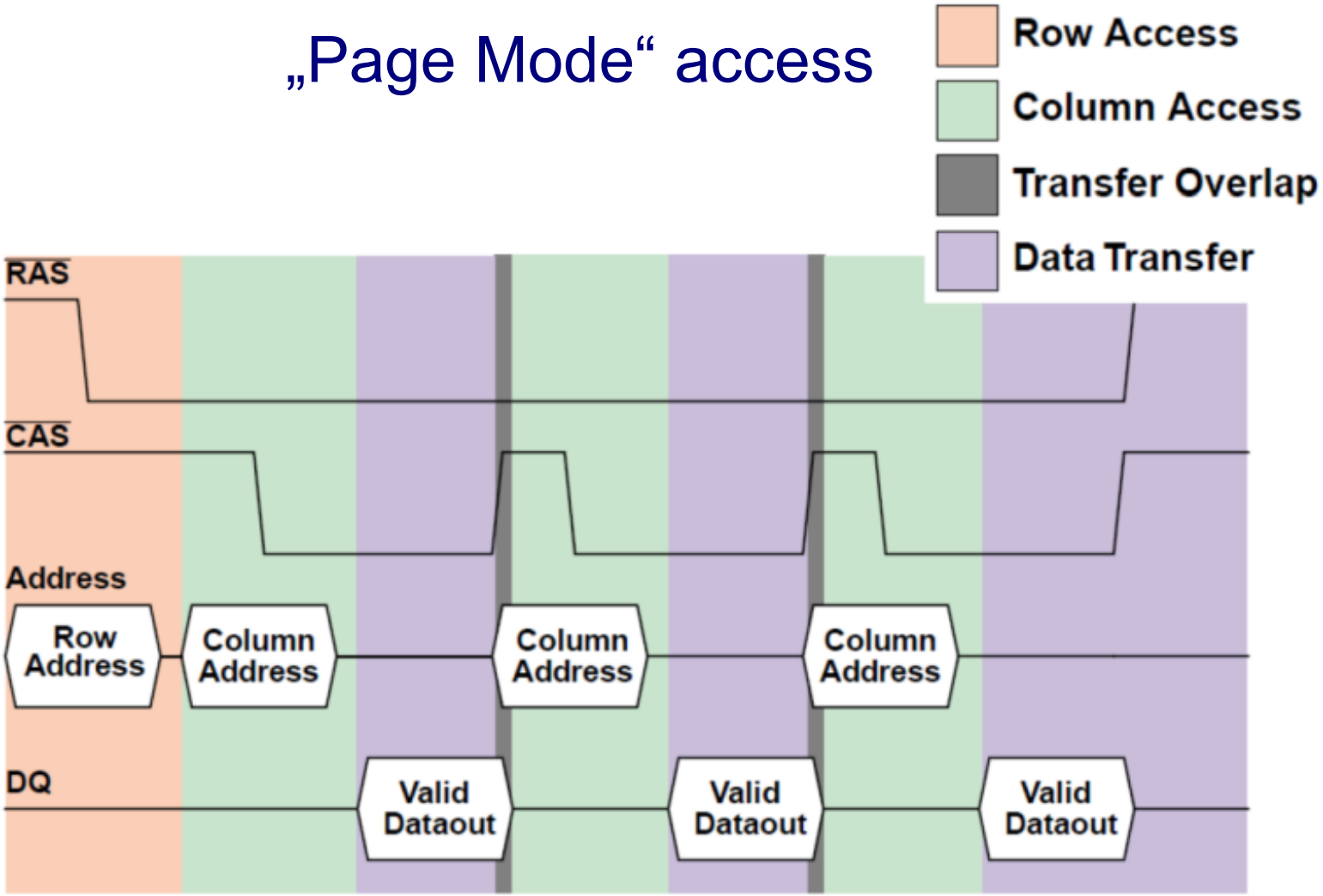
Async. DRAM – Timing for Read operation

Random Access



Async. DRAM – Timing for Read operation

„Page Mode“ access



- Comparison of SRAM and DRAM memory cells‘ properties:
  - Content in both SRAM and DRAM cells, is unstable (volatile) on the interruption of the power supply
  - DRAM cell is simpler (one transistor), and smaller in size
    - cell density per unit area of the chip is therefore the DRAM significantly greater than for SRAM
    - The price is lower than that of SRAM memories
  - DRAM cells require periodic refresh of the content, which requires special refresh circuit; SRAM cells do not have this requirement.

- SRAM memory cell are faster (switching transistor) as a DRAM (charging the capacitor)

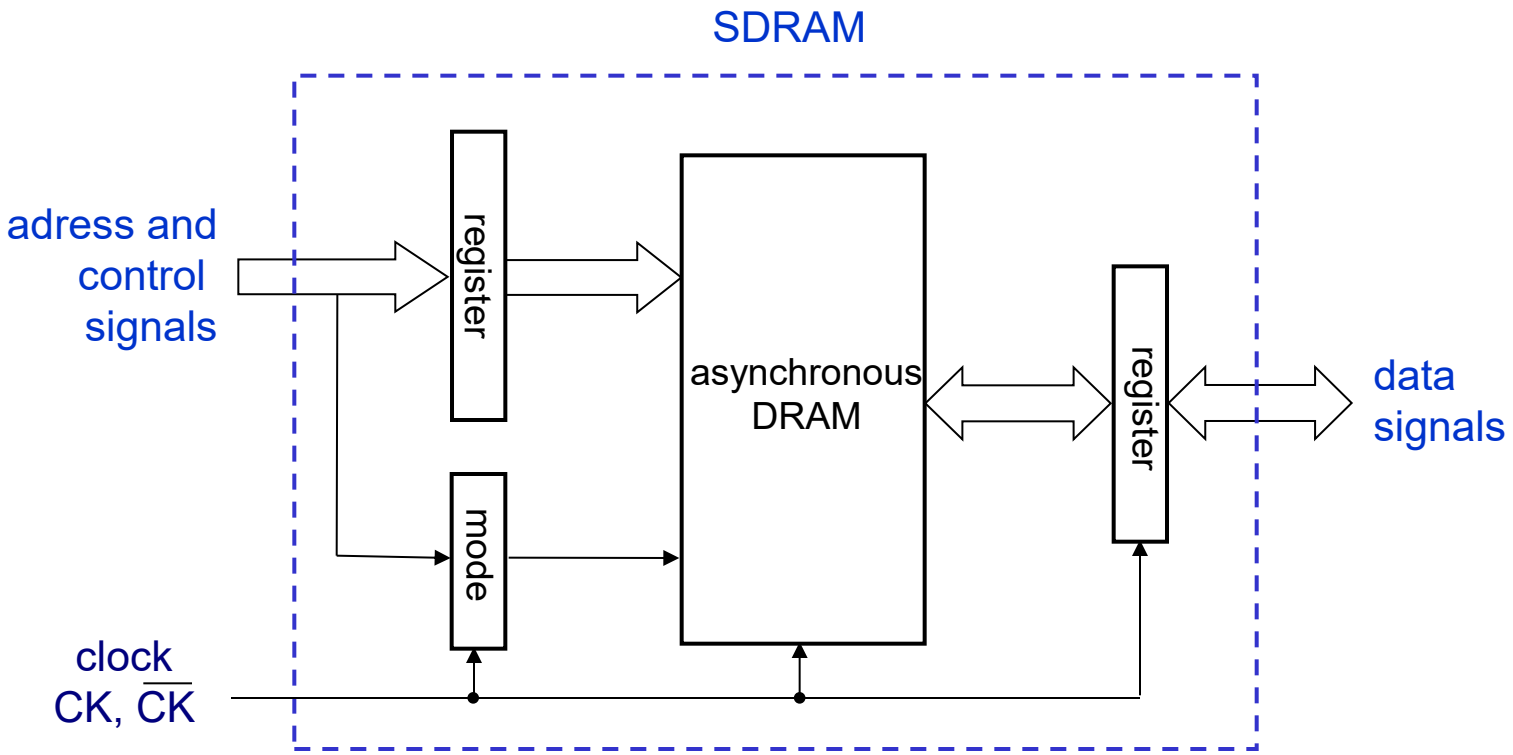
- DRAM memory are as a result of lower cost and higher density (more bits per chip) used for the large memories, e.g. the main memory.

- SRAM memory, due to faster speeds and higher prices are used for small memories that are primarily caches.

8.2.3 SDRAM - Synchronous Dynamic RAM

- Conventional DRAMs are today called asynchronous.
- Synchronous DRAMs are made in the form of a simple pipeline, so they require clock signal for the operation.
- The basis of the SDRAM is asynchronous DRAM with added registers, in which the active front clock signal stores address, control and data signals.
- The request for the next access can be sent to the SDRAM even when the DRAM is still busy with the execution of previous access.

- The time of the first access is the same as for asynchronous DRAMs, following accesses are faster.



- On „page-mode“ access to bits in the same row, SDRAM is much faster than asynchronous, since the access request is stored in the registers during the execution of the previous access.
- SDRAMs are in production since 1993, the development phases are denoted as DDR, DDR2, DDR3 and DDR4.
- Features of SDRAMs are standardized, standards are issued by organization JEDEC (Joint Electron Devices Engineering Council).
- After 2000, the computers use only Synchronous DRAMs (SDRAM).

- Overview of DDRx memories

DDR SDRAM Standard	Internal rate (MHz)	Bus clock (MHz)	Prefetch	Data rate (MT/s)	Transfer rate (GB/s)	Voltage (V)
SDRAM	100-166	100-166	1n	100-166	0.8-1.3	3.3
DDR	133-200	133-200	2n	266-400	2.1-3.2	2.5/2.6
DDR2	133-200	266-400	4n	533-800	4.2-6.4	1.8
DDR3	133-200	533-800	8n	1066-1600	8.5-14.9	1.35/1.5
DDR4	133-200	1066-1600	8n	2133-3200	17-21.3	1.2
DDR5	200-400	1600-3200	16n	3200-6400	25.6-51.2	1.1

Source: https://www.transcend-info.com/Support/FAQ-296

- Overview of DDRx memories

			Best case access time (no precharge)			Precharge needed
Production year	Chip size	DRAM type	RAS time (ns)	CAS time (ns)	Total (ns)	Total (ns)
2000	256M bit	DDR1	21	21	42	63
2002	512M bit	DDR1	15	15	30	45
2004	1G bit	DDR2	15	15	30	45
2006	2G bit	DDR2	10	10	20	30
2010	4G bit	DDR3	13	13	26	39
2016	8G bit	DDR4	13	13	26	39

Figure 2.4 Capacity and access times for DDR SDRAMs by year of production. Access time is for a random memory word and assumes a new row must be opened. If the row is in a different bank, we assume the bank is precharged; if the row is not open, then a precharge is required, and the access time is longer. As the number of banks has increased, the ability to hide the precharge time has also increased. DDR4 SDRAMs were initially expected in 2014, but did not begin production until early 2016.

source: Henn.-Patt: Computer Architecture: A Quantitative Approach

Overview of DDRx memories

Standard	I/O clock rate	M transfers/s	DRAM name	MiB/s/DIMM	DIMM name
DDR1	133	266	DDR266	2128	PC2100
DDR1	150	300	DDR300	2400	PC2400
DDR1	200	400	DDR400	3200	PC3200
DDR2	266	533	DDR2-533	4264	PC4300
DDR2	333	667	DDR2-667	5336	PC5300
DDR2	400	800	DDR2-800	6400	PC6400
DDR3	533	1066	DDR3-1066	8528	PC8500
DDR3	666	1333	DDR3-1333	10,664	PC10700
DDR3	800	1600	DDR3-1600	12,800	PC12800
DDR4	1333	2666	DDR4-2666	21,300	PC21300

Figure 2.5 Clock rates, bandwidth, and names of DDR DRAMS and DIMMs in 2016. Note the numerical relationship between the columns. The third column is twice the second, and the fourth uses the number from the third column in the name of the DRAM chip. The fifth column is eight times the third column, and a rounded version of this number is used in the name of the DIMM. DDR4 saw significant first use in 2016.

source: Henn.-Patt: Computer Architecture: A Quantitative Approach

- Evolution of SDRAM memories (2017+)

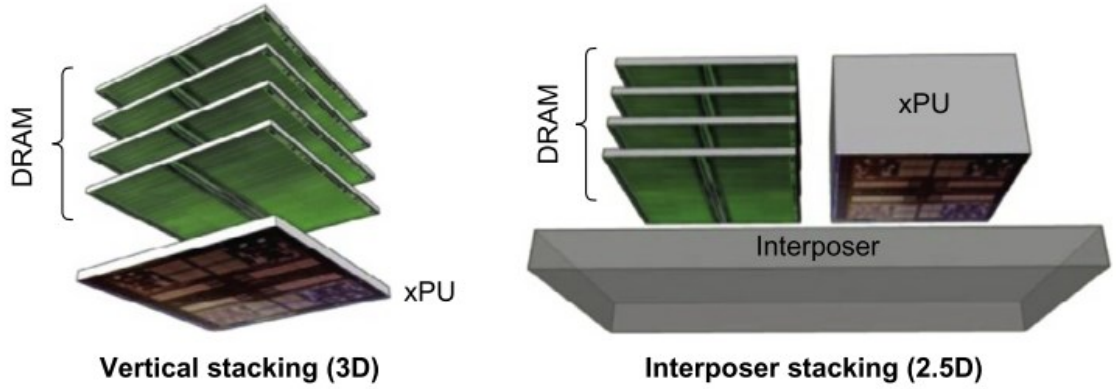


Figure 2.7 Two forms of die stacking. The 2.5D form is available now. 3D stacking is under development and faces heat management challenges due to the CPU.

Packaging Innovation: Stacked or Embedded DRAMs

[Patt]

The newest innovation in 2017 in DRAMs is a packaging innovation, rather than a circuit innovation. It places multiple DRAMs in a stacked or adjacent fashion embedded within the same package as the processor. (Embedded DRAM also is used to refer to designs that place DRAM on the processor chip.) Placing the

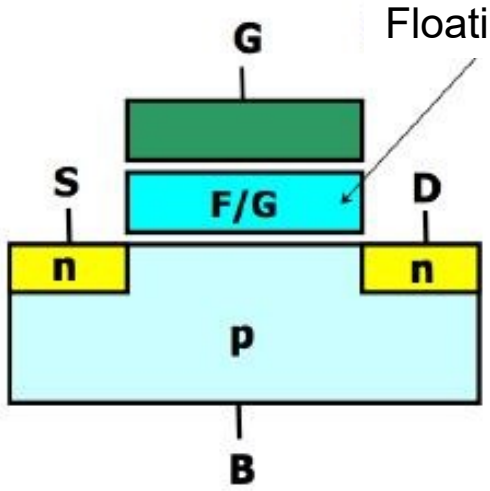
source: Henn.-Patt: Computer Architecture: A Quantitative Approach

8.2.4 Flash memory

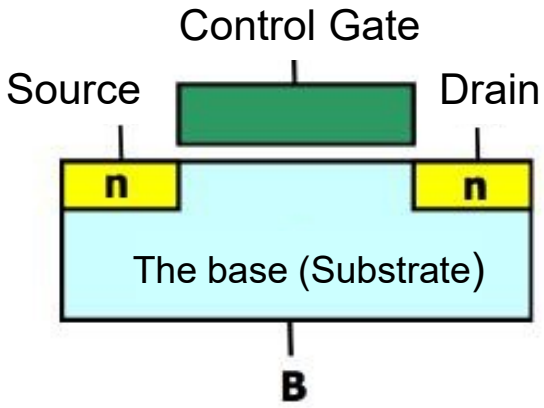
- Flash memory is a type of electrically erasable semiconductor read-only memory (EEPROM - Electrically erasable Programmable Read only Memory), which retains its contents even after turning off the power supply.
- Before we can write in flash memory cell, we must erase their content. With one quick operation, a large area of data (block) is erased, hence the name flash memory.
- The number of deletions is limited to 3,000 to 100,000, depending on the type of memory cell.
- Erased memory cells have a content of 1 (value 1)
- Writing is similar to EEPROM, it modifies values of 1 to zeros, where needed.

Structure and operation of flash memory cell

- Flash memory cell is similar to a MOS FET transistor, except that it has an additional floating gate, which can store electrical charge (electrons).
- Flash memory cell = FGMOS (Floating Gate MOS) transistor

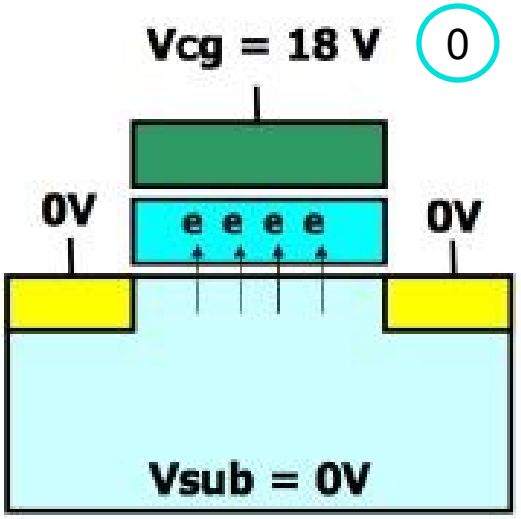


Flash memory cell
FGMOS transistor



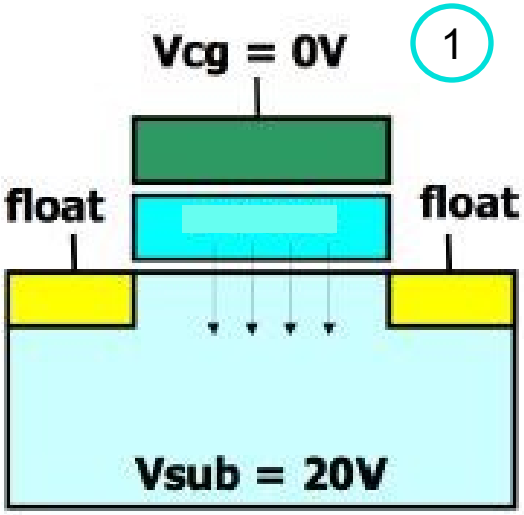
MOSFET transistor

- Writing and erasing



Writing → State 0

A positive voltage on the control gate causes transition of electrons to the floating gate (tunneling current through an oxide insulation layer)



Delete → State 1

The positive voltage at the substrate frees electrons from the floating gate.

- Depending on the number of bits that can be stored in one flash memory cell (one transistor), we have currently three types of cells:
  - SLC (Single-Level Cell) - 1 bit per cell - 2 states of charge in floating gate
  - MLC (Multi-Level Cell) - 2 bits per cell - 4 states of charge
  - TLC (Triple-Level Cell) - 3 bits per cell - 8 states of charge

- SLC (Single-Level Cell)
  - One SLC cell is capable of storing 1 bit of information (two states i.e. two levels of charge in the floating gate)
  - Lower density (1 bit per cell)
  - Up to 100,000 erase/write cycles per cell
  - Lower energy consumption, faster writing
  - Higher price

- MLC (Multi-Level Cell)
  - One MLC cell can store two bits of information, implying 4 states, and 4 levels of charge in the floating gate.
  - Higher density (2 bits per cell)
  - Up to 10,000 erase/write cycles per cell
  - Shorter life span than SLC
  - Low price (3-fold lower than SLC)

- TLC (Triple-Level Cell)
  - One TLC cell can store three bits of information, 8 states i.e. 8 levels of charge in the floating gate.
  - Higher density (3 bits per cell)
  - Up to 5000 erase/write cycles of the cell
  - Shorter life span than MLC and SLC
  - Lower cost (30% lower than the MLC)

- During the transition of electrons from the floating gate into the substrate, and vice versa an intermediate insulating oxide layer of collapse.
- The number of deletions (or delete-write cycles), is therefore limited. Any typeflash memory cells has a maximum number of wiping cycles.
  - SLC memory cell to 100,000
  - MLC pmnilniška cell to 10,000
  - TLC memory cell to 5,000

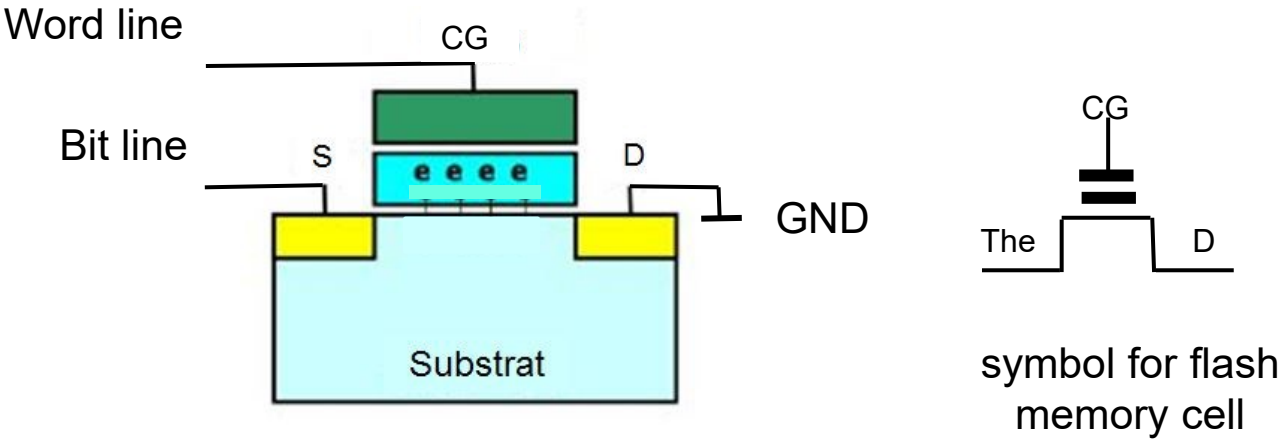
- Comparison of three basic types of cells:

Features	SLC (Single-Level Cell)	MLC (Multi-Level Cell)	TLC (Triple-Level Cell)	QLC (Quad-Level Cell)
bits/cell	1	2	3	4
price	higher	3xnižja from SLC	1/3 lower than MLC	lowest
no. E/W cycles	100000	10000	5000	1 000
Durability		less than SLC	shorter	shortest
Others	lower consumption, fast writing			3D NAND

SSD disks

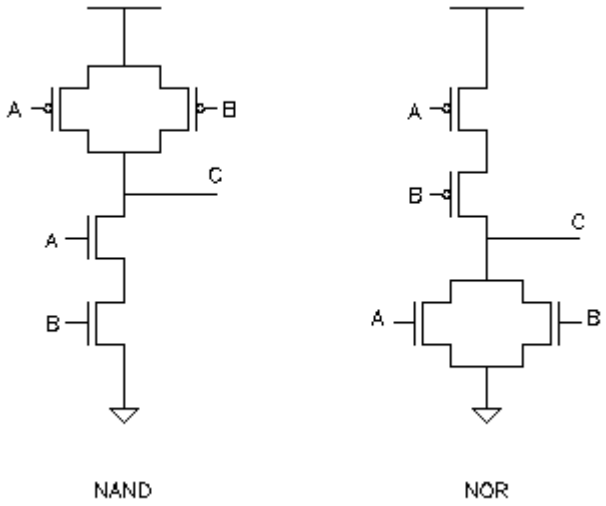
Connecting memory cells in flash memory

- The connections of the memory cells in flash memories is quite different from e.g. RAM memory.

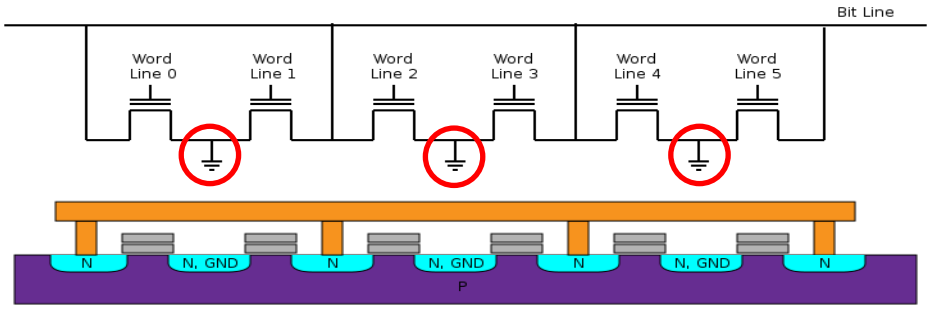


- According to the connections of memory cells, there are two types flash memory:
  - NOR flash memory
  - NAND flash memory

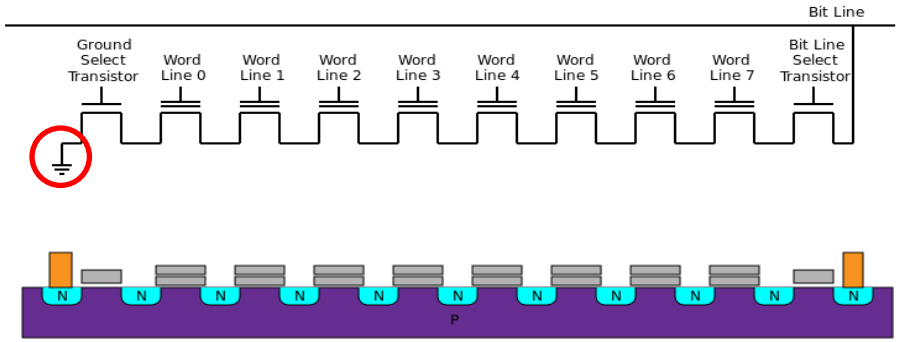
- The names are derived from the similarity with connections of the transistors in NOR or NAND gates.



- NOR flash memory



- NAND flash memory



NOR flash memory:

- each memory cell is connected to the bit line, and source line.
- random access to bytes (program memory)

+ Each cell is addressable, fast reading
- more complex structure, slow writing

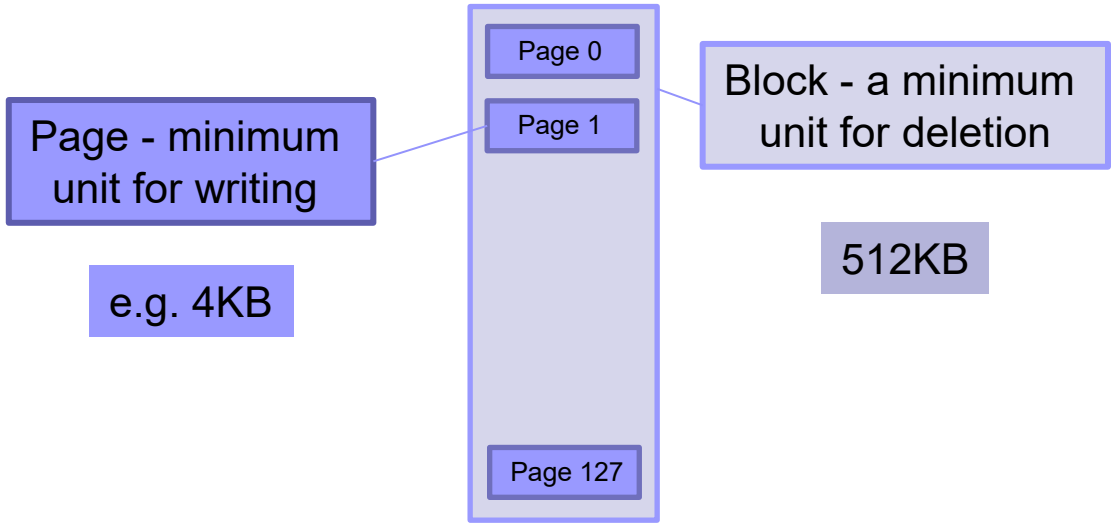
NAND flash memory:

- more memory cells connected in series and you share the bit line - smaller number of lines on chip
- random access to pages (auxiliary memory. - disk)

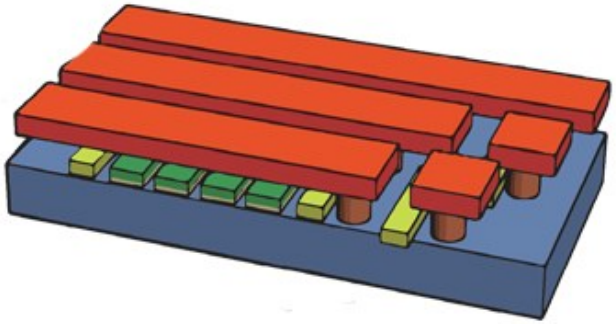
+ higher density, lower price, fast writing
- slow reading

Attribute	NAND	NOR
Main application	File storage	Code execution
Storage capacity	High	Low
Cost per bit	Better	
Active power	Better	
Standby power		Better
Write speed	Good	
Read speed		Good

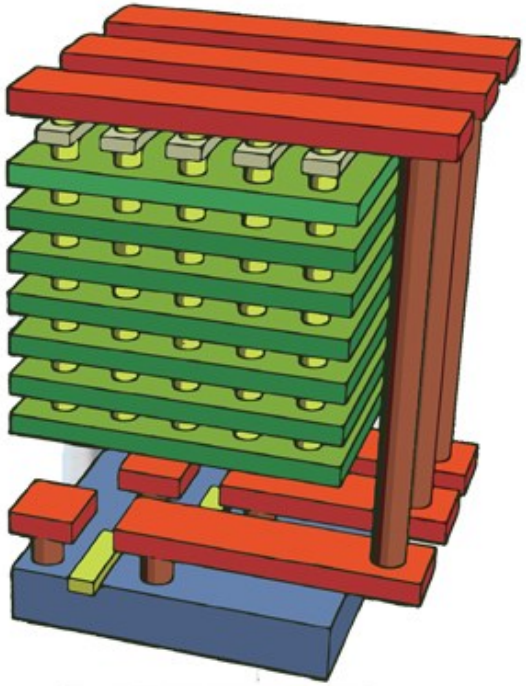
- NAND flash memories are divided into pages, which are typically 4 or 8 KB.
- Multiple pages (typically 64 or 128 pages) form a block.
- The smallest writable unit is the page, the smallest unit of erasing is the block.
- Before writing the page, it has to be erased.



- 3D NAND flash memories :



2D NAND



3D NAND

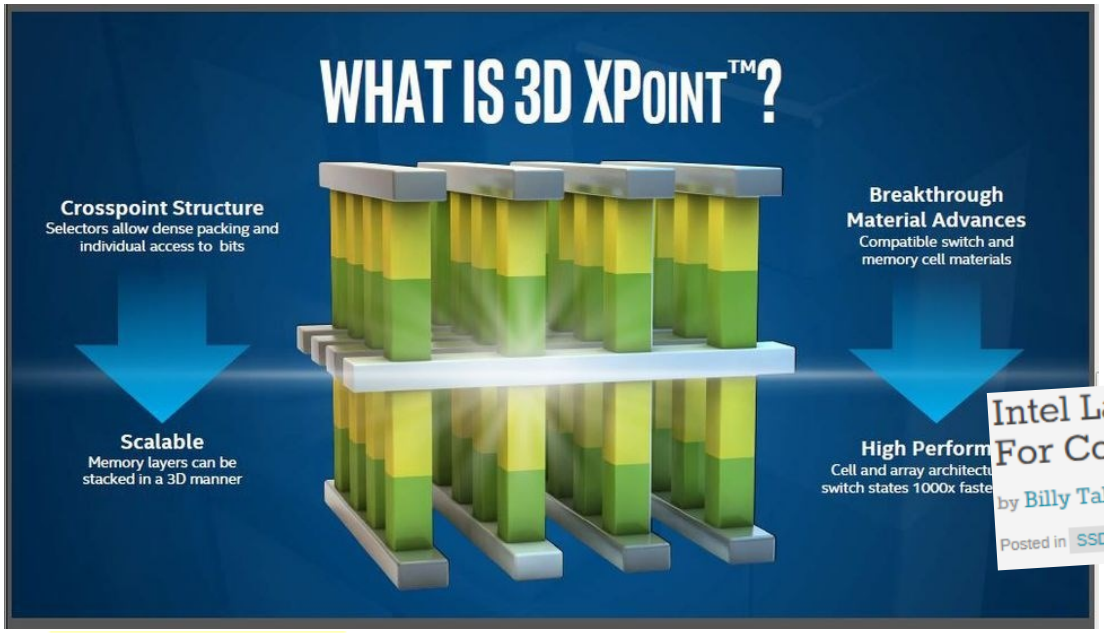
Tuesday, May 15th 2018

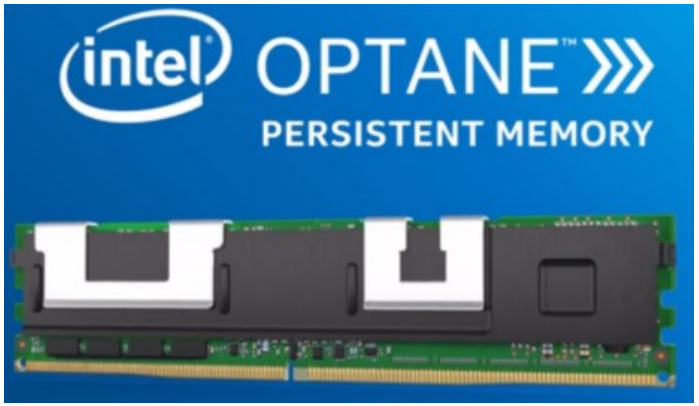
International Memory Workshop: 3D NAND Flash to Reach 140 Layers By 2021

by Raevenlord | May 15th, 2018 18:50 | Discuss (11 Comments)

Phase-Change Memory - PCM

- **3D Xpoint (Intel, Micron) – tudi „memristor“**





Intel Launches Optane Memory M.2 Cache SSDs For Consumer Market

by Billy Tallis on March 27, 2017 12:00 PM EST

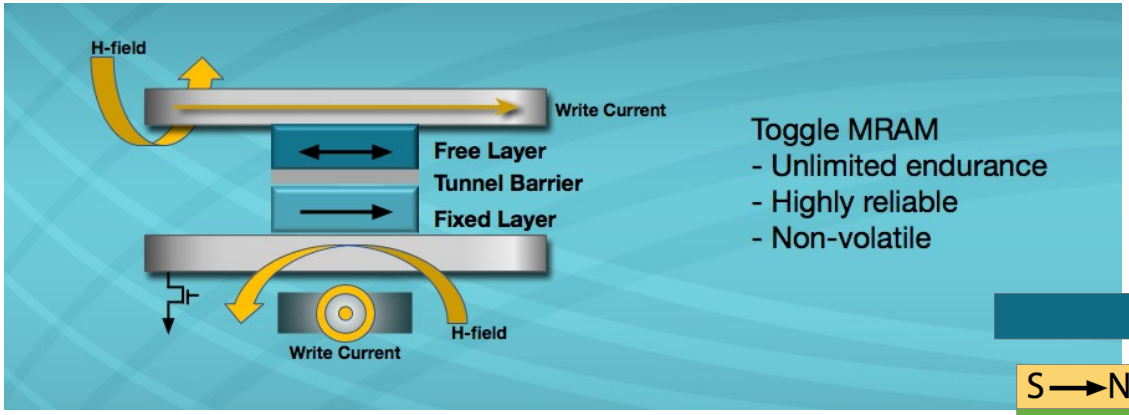
Posted in SSDs Storage Intel SSD Caching M.2 NVMe 3D XPoint Optane Optane Memory

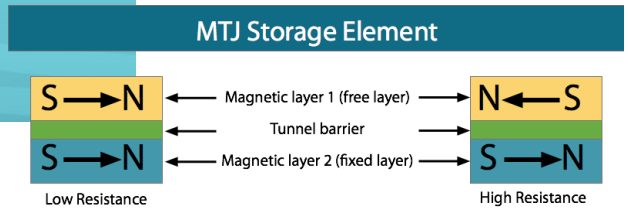
In 2017 Micron and Intel began delivering Xpoint memory chips that are believed to be based on PCM. The technology is expected to have much better write durability than NAND Flash and, by eliminating the need to erase a page before writing, achieve an increase in write performance versus NAND of up to a factor of ten. Read latency is also better than Flash by perhaps a factor of 2–3. Initially, it is expected to be priced slightly higher than Flash, but the advantages in write performance and write durability may make it attractive, especially

[Patt]

Toggle MRAM Technology

- **MRAM - Magnetoresistive random-access memory**





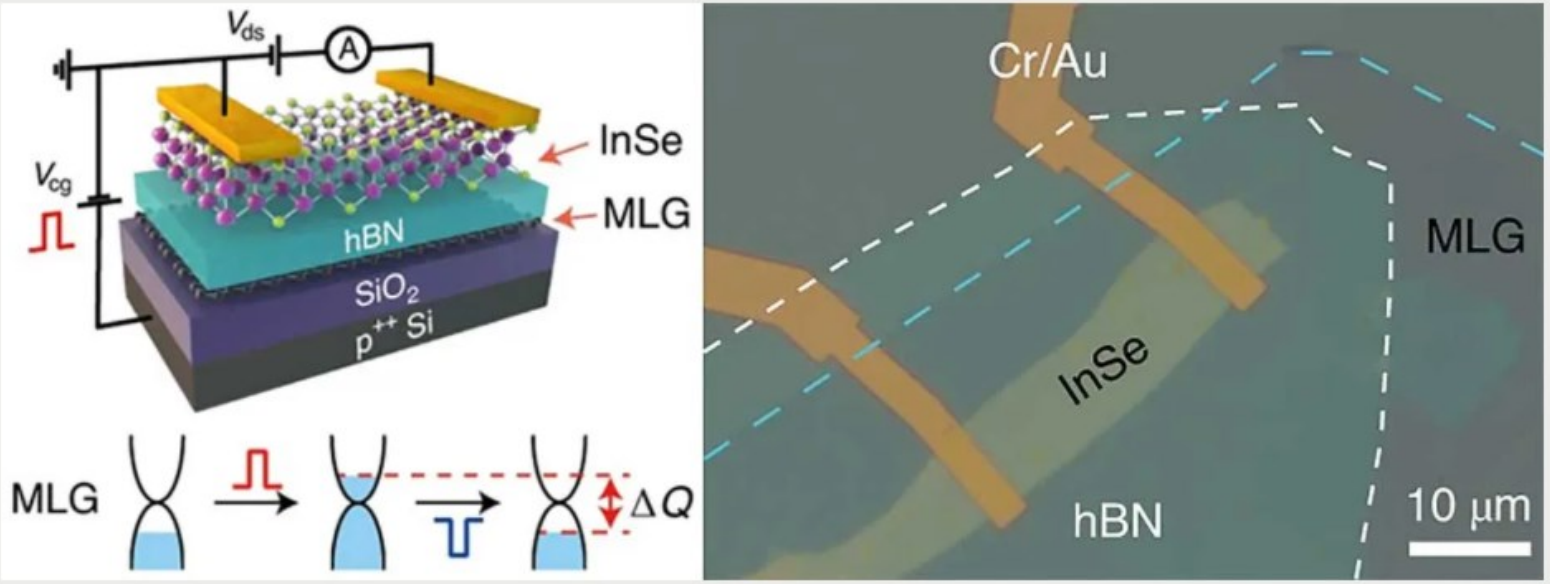
Toggle MRAM Characteristics	
NON-VOLATILE	Data retention > 20 years
FAST	Symmetrical read/write - 35ns
UNLIMITED ENDURANCE	No wear-out mechanism
MODULAR INTEGRATION	Easily integrated with CMOS
EXTENDED TEMPERATURES	-40c < T < 150C operation demonstrated
HIGHLY RELIABLE	Intrinsic reliability exceed 20 year lifetime at 125C

NEWS | COMPUTING

Flash Memory's 2D Cousin is 5,000 Times Speedier ›

New memory could be multi-bit for ultra-high-density storage

BY CHARLES Q. CHOI | 14 MAY 2021 | 2 MIN READ |

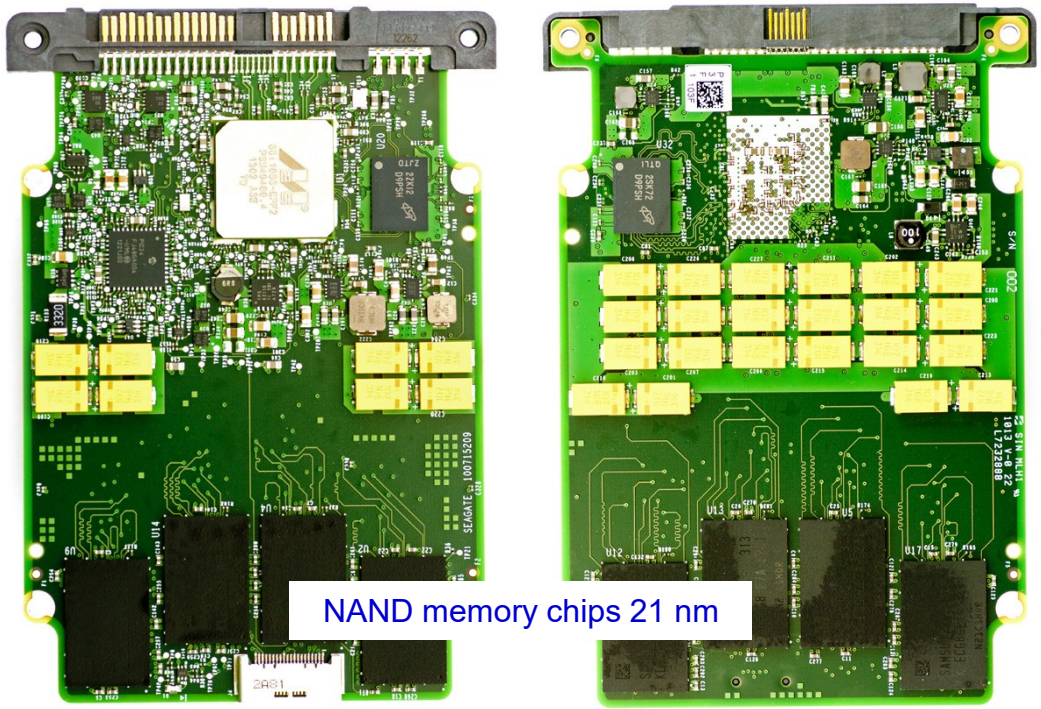


Two-dimensional indium selenide-based floating-gate memory device IMAGE: NATURE NANOTECHNOLOGY

Solid State Drives - SSD

- Disks based on flash memories are the first serious competitor to the magnetic disks.
- SSD (Solid State Drive) units are the auxiliary (secondary) memories, which represent a replacement for the HDD (magnetic disk).
- The SSD disks use NAND flash MLC or TLC memory cells.
- The external interface is commonly SATA 3.0, SATA or PCIe.

Seagate 1200 SSD 400GB



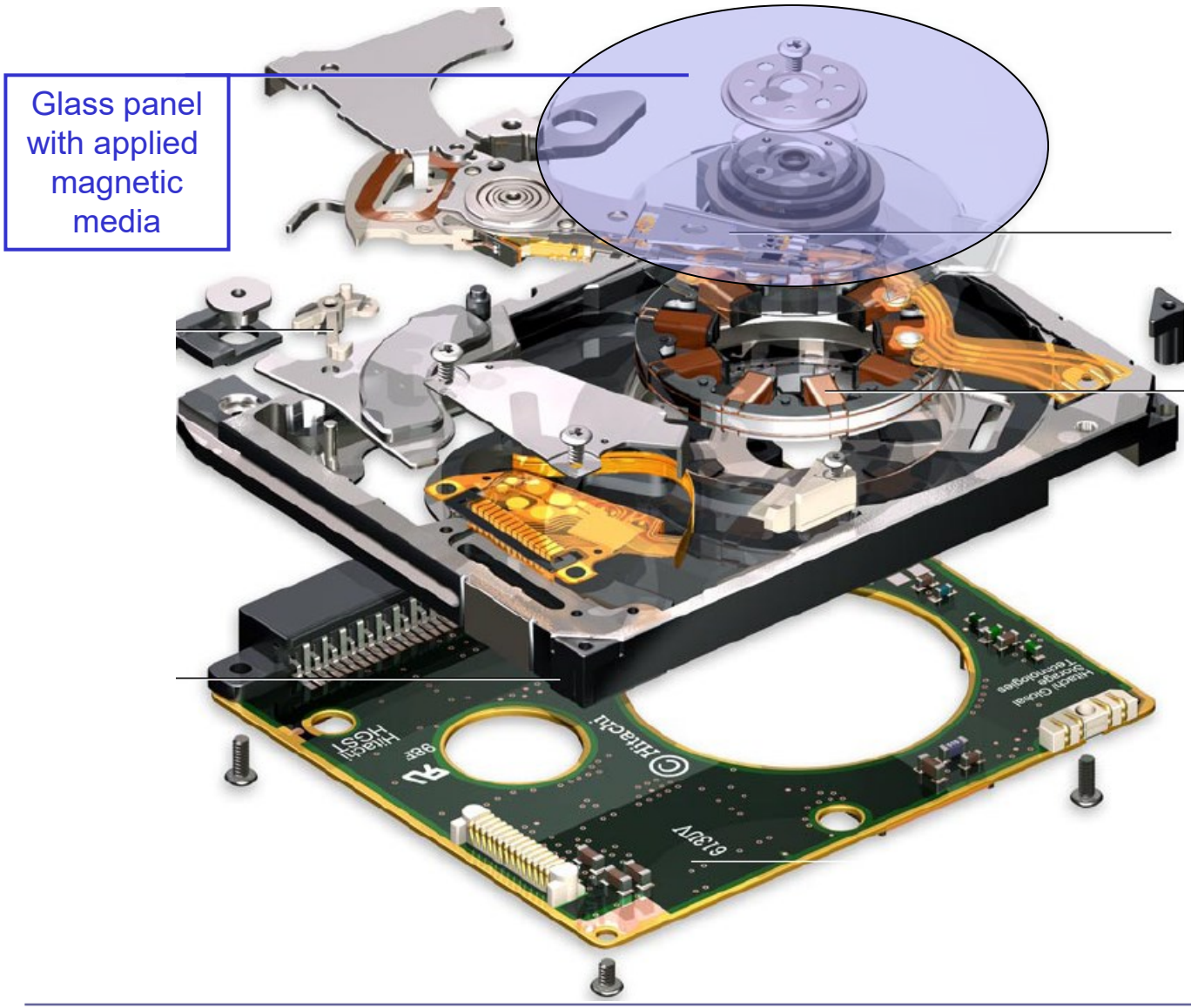
Upper Side Bottom Side

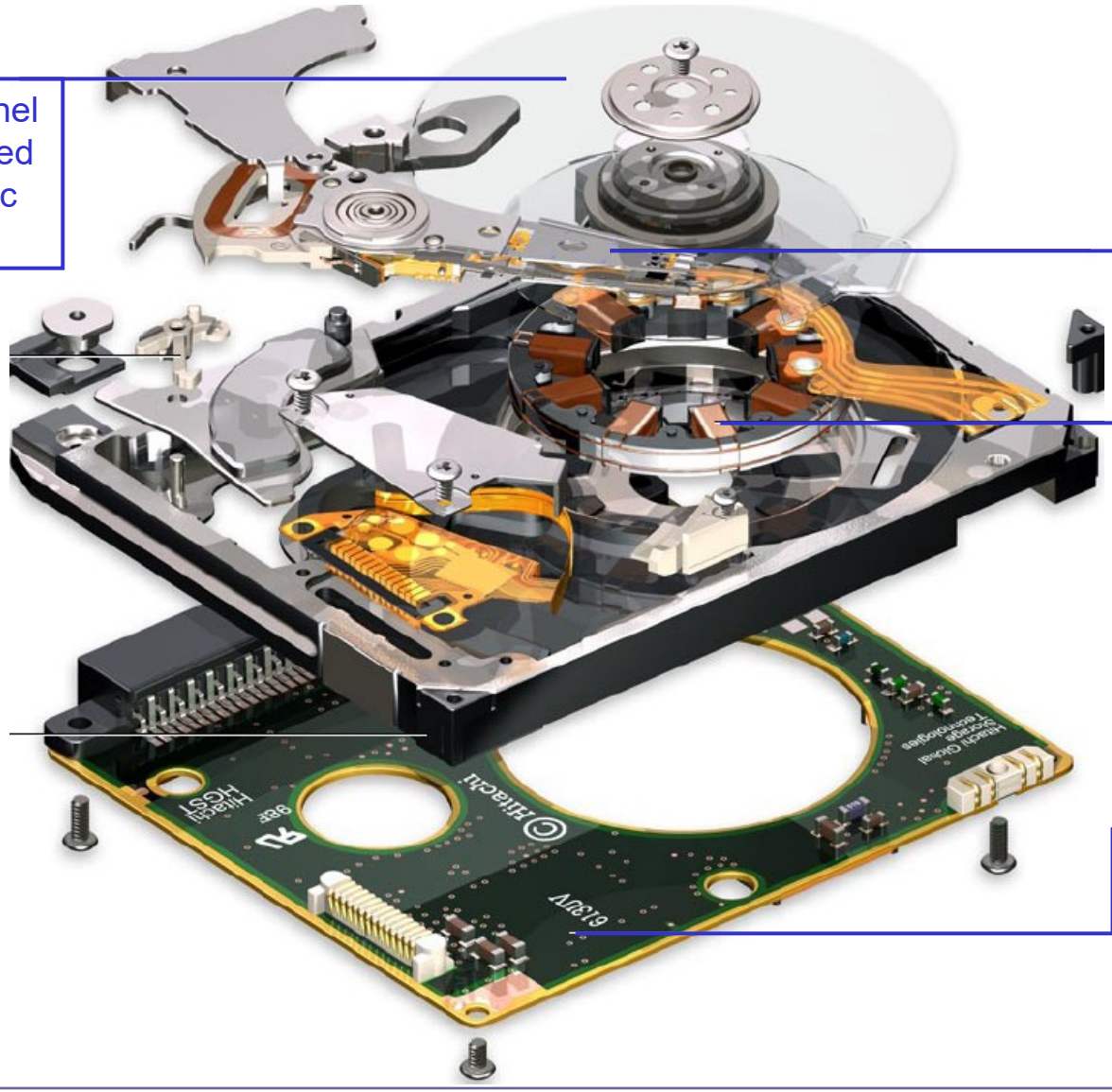
of printed circuit board

http: //www.storagereview.com/seagate_1200_enterprise_ssd_review

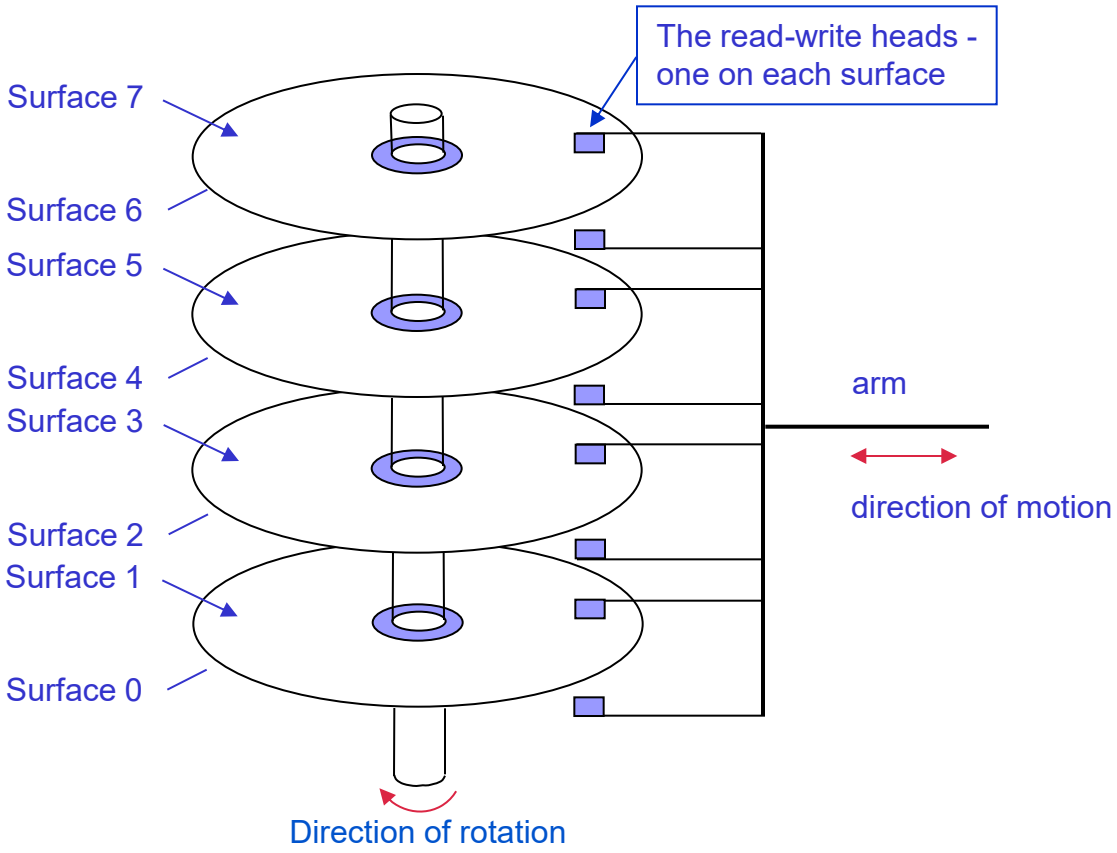
8.2.5 HDD - magnetic disk

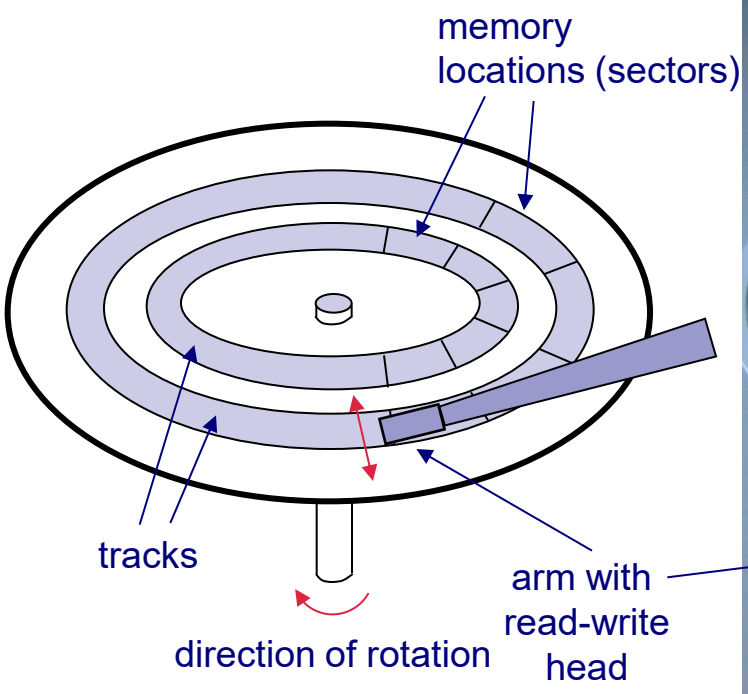
- Magnetic disk is from 1956 the most important type of auxiliary memory.
- Direct access - a combination of sequential and circular access.
- Components:
  - Disks with magnetic media and motor drive boards. The disks rotate with a constant number of revolutions.
  - Handles with read-write heads
  - Electronics for reading and writing
  - Electromechanical servo motor and a control system for positioning of read-write heads on the track
  - The controller and the interface to the bus

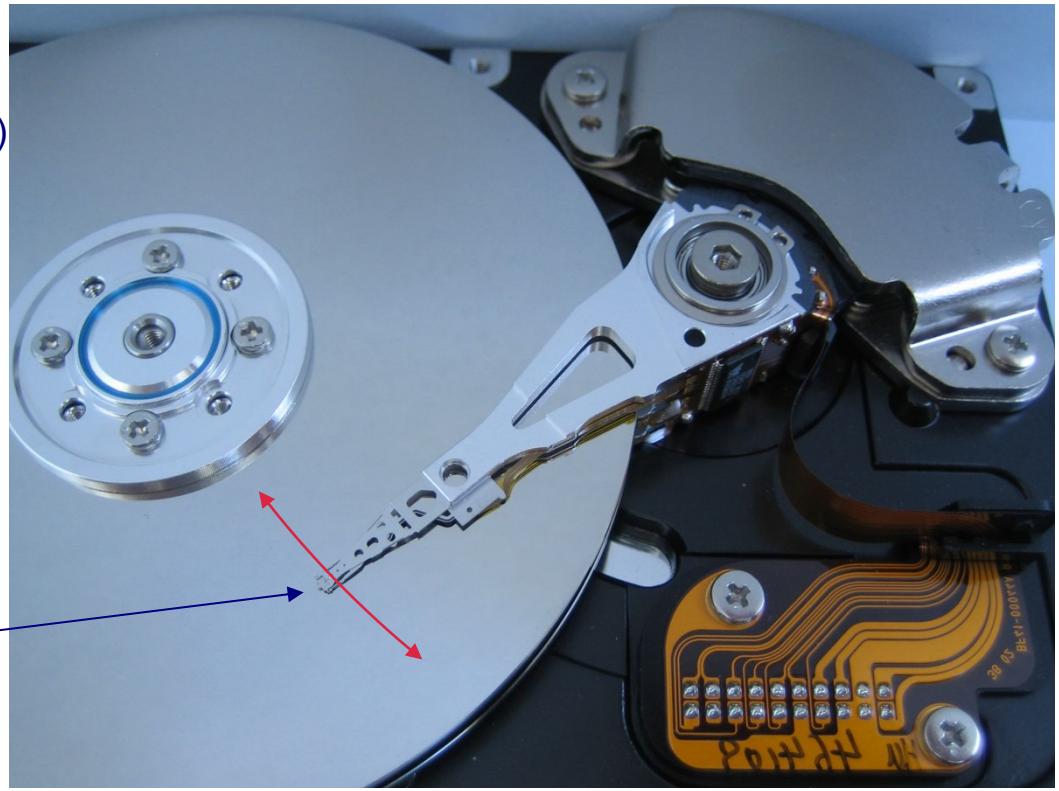




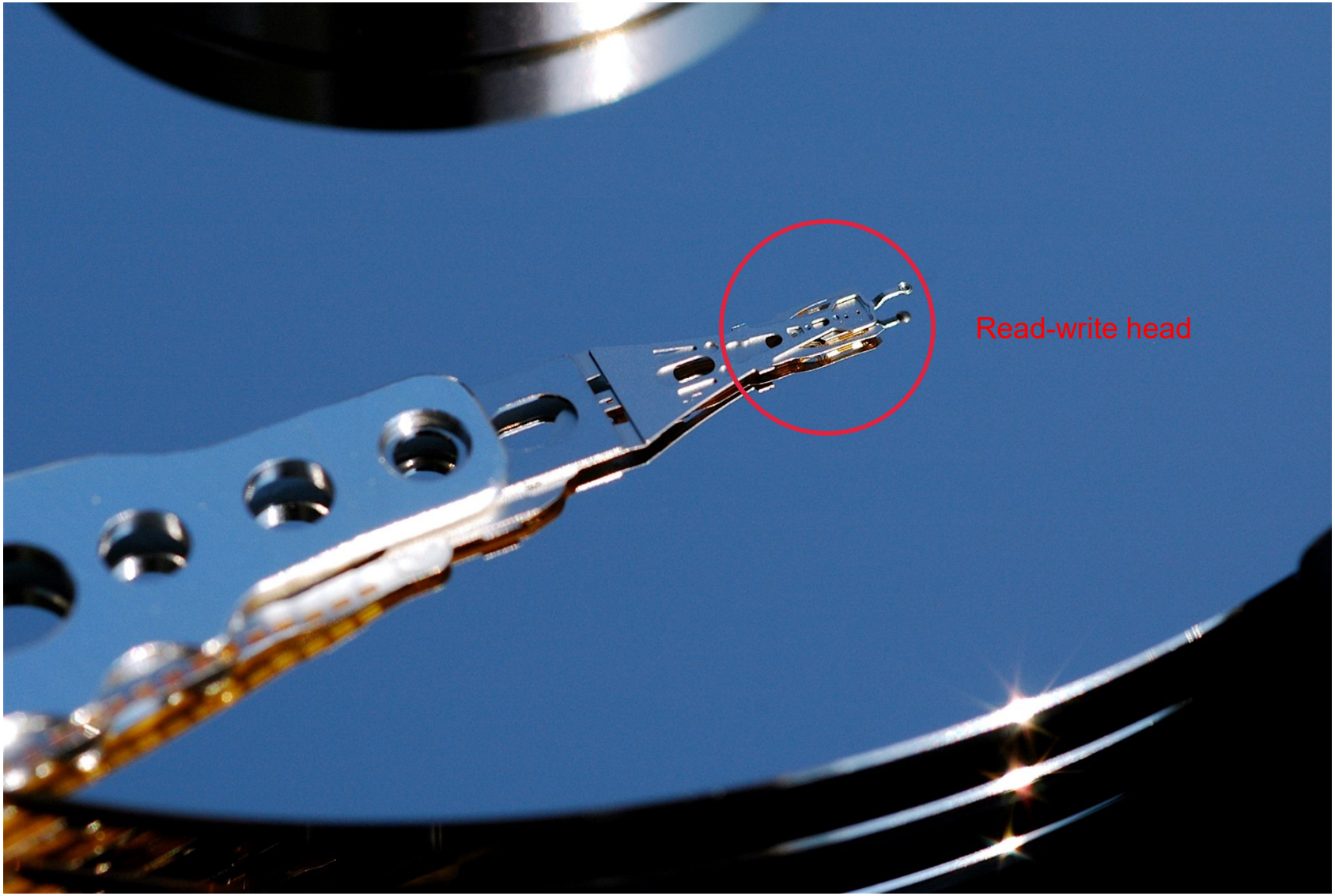
Magnetic disk drive with four plates and eight surfaces - scheme

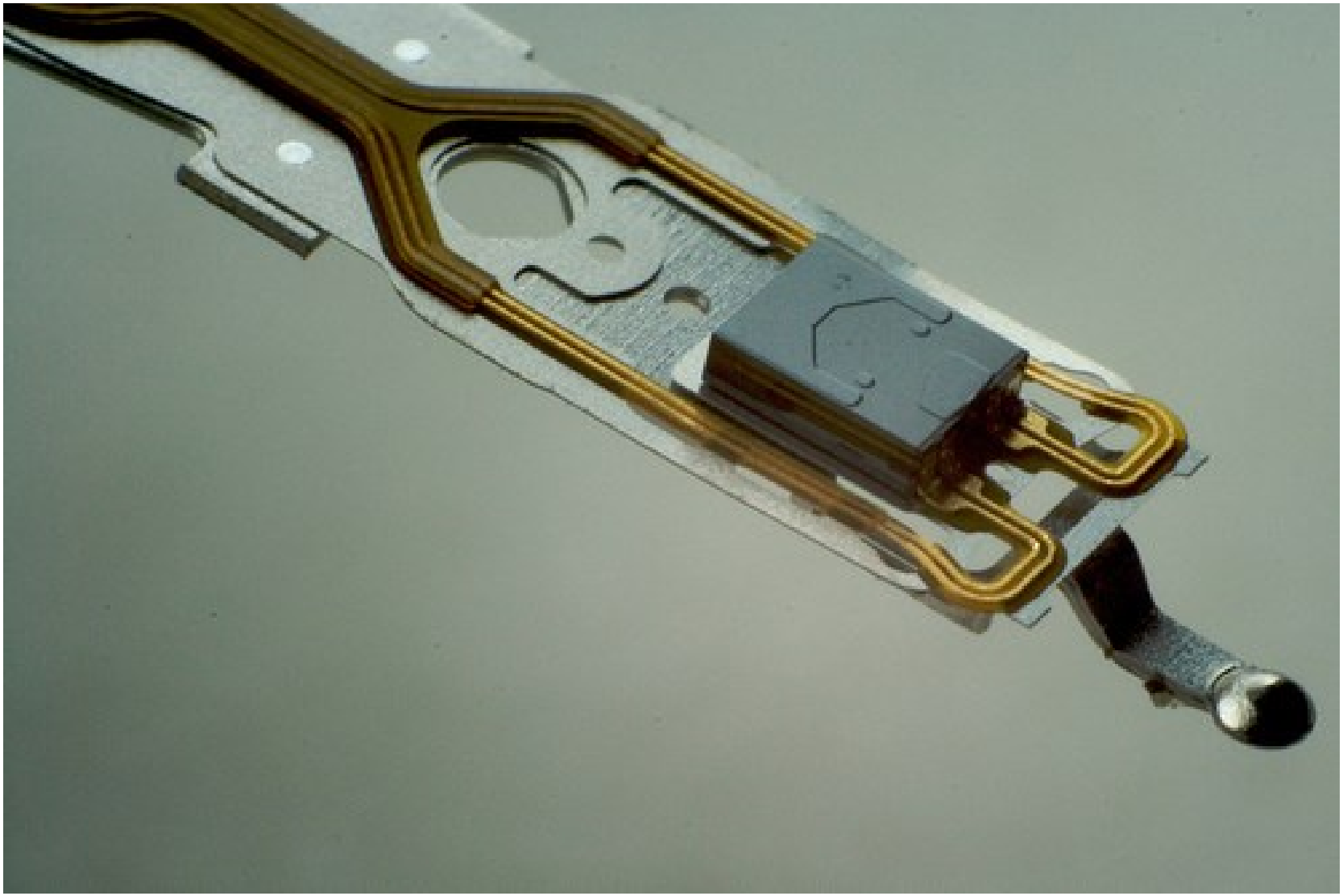




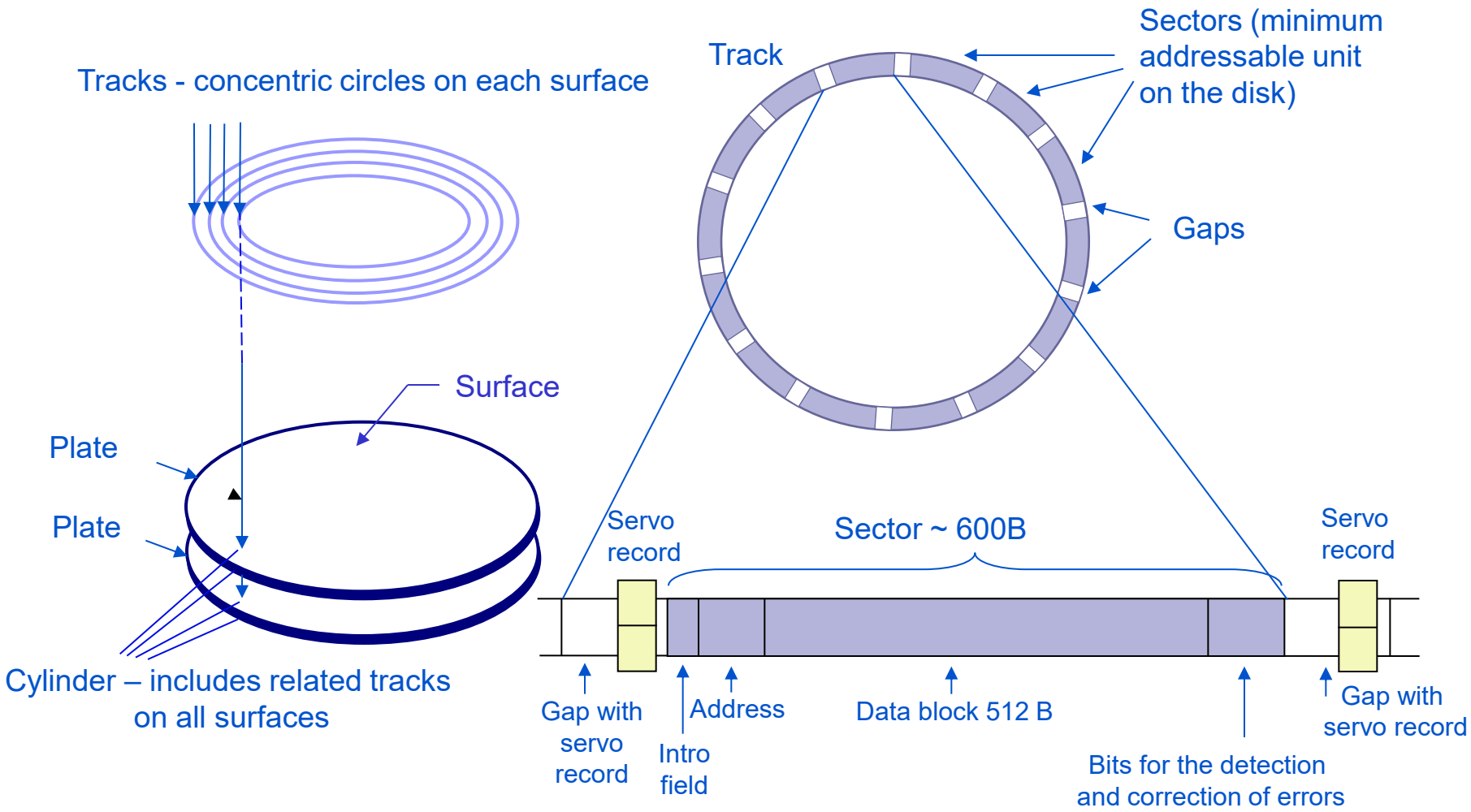


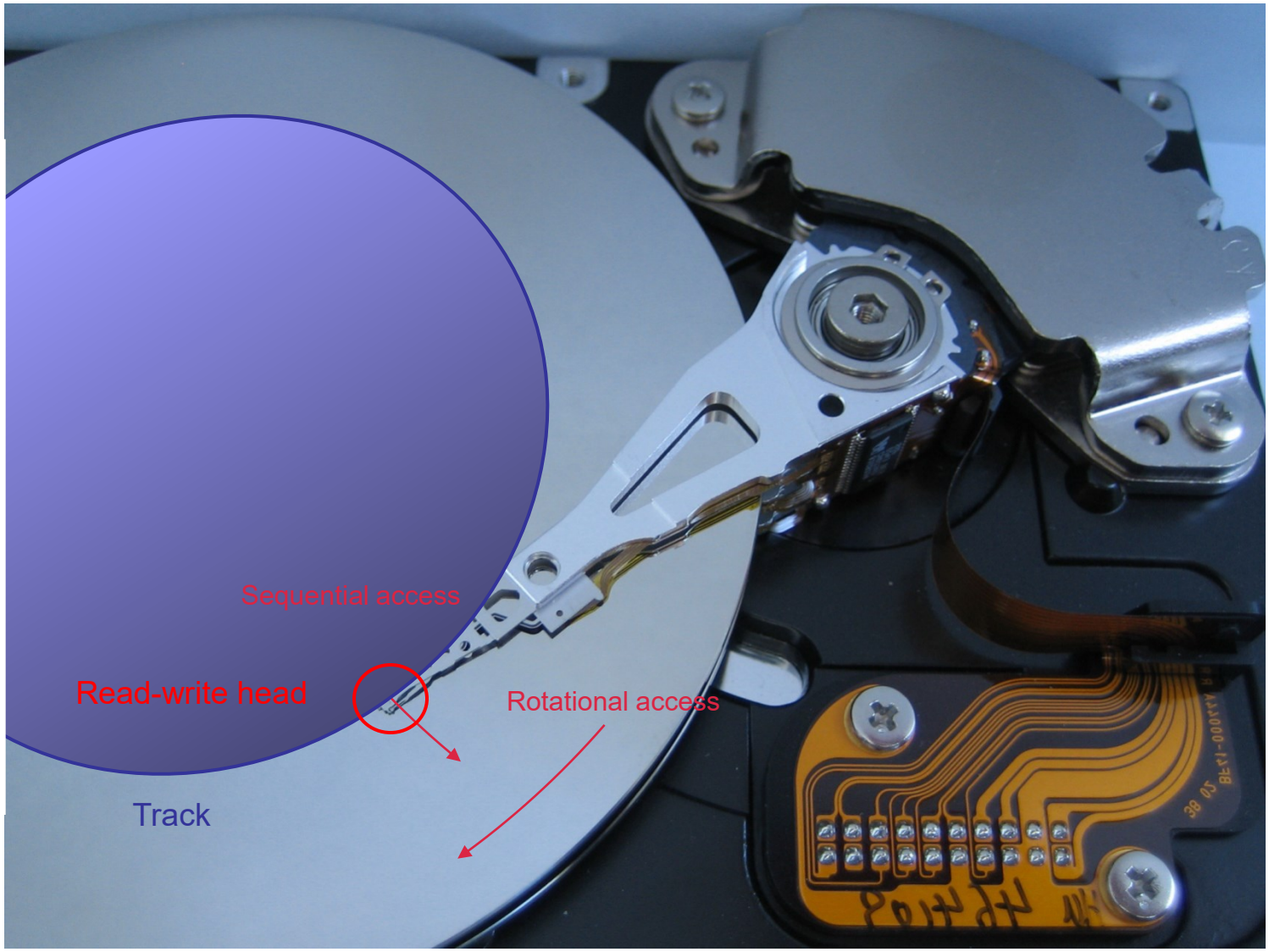
© MMI





Organization of data on disk




Sequential access
Read-write head
Rotational access
Track

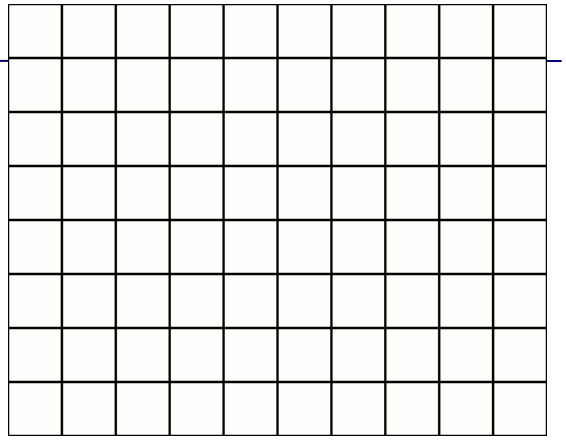
- Access to a sector on the disk consists of three steps:

t_{SEEK}
- Search track - sequential access - movement of the head to a desired track (cylinder)
  - Average search time is 2 - 10 ms

t_{LAT}
- Rotational delay (latency) - the average rotational latency is ½ the time of one revolution
  - At 5400 rpm, latency is 5.56 ms
  - At 7200 rpm, latency is 4.167 ms
  - At 15000 rpm, latency is 2 ms

t_{SECT}
- Data transfer
  - The transfer time depends on the internal transfer speed and the number of transferred sectors

- Time for access to the sector is the sum of all of the three times and is usually 3 to 15 ms



By XZise - Own work, CC BY-SA 3.0,
https://commons.wikimedia.org/w/index.php?curid=4128212

Case- read of a file with 10 sectors:

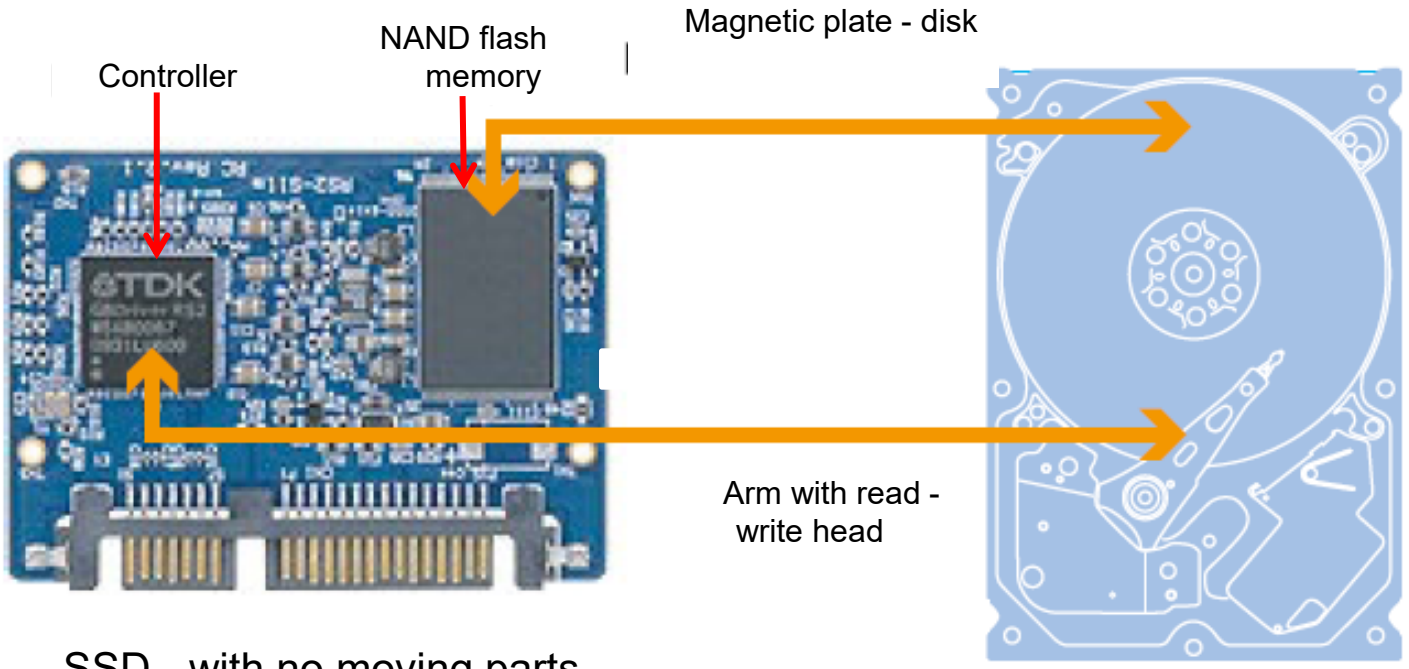
1. Non-fragmented file (consecutive sectors on same track)

$$T_{dat1} = t_{SEEK} + t_{LAT} + 10\, t_{SECT}$$

2. Fragmented file (each sector on different track)

$$T_{dat2} = 10 * (t_{SEEK} + t_{LAT} + t_{SECT})$$

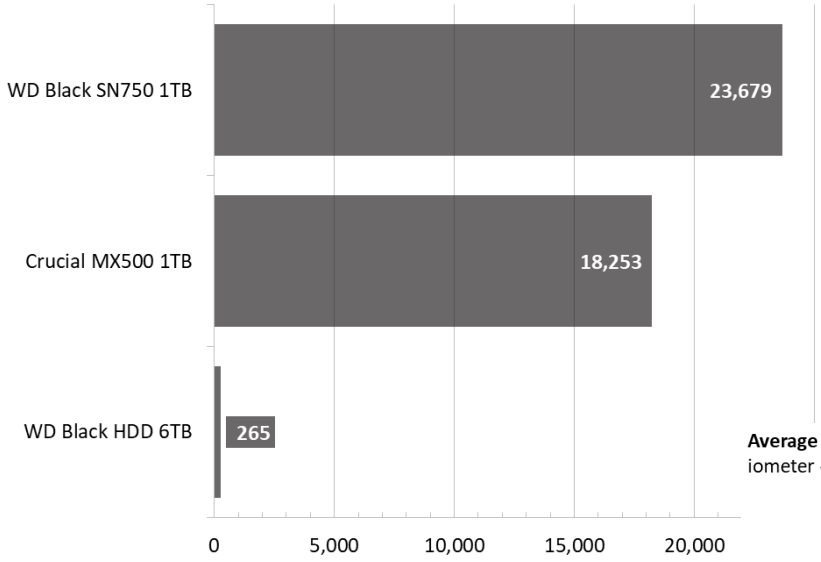
8.3 Comparison of SSD and HDD



Comparison of SSD and HDD

Average Random Read - 4KB QD1-4
iometer - IOPS - Higher is Better

tom's HARDWARE

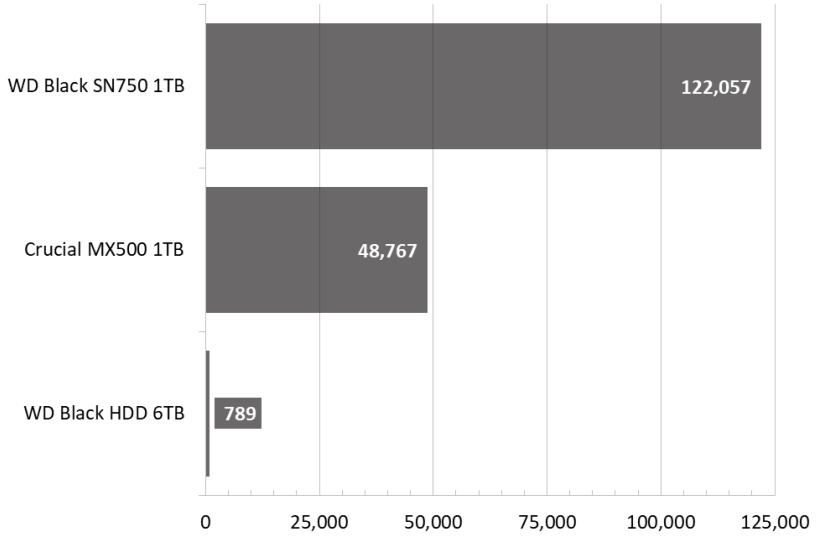


Comparison :

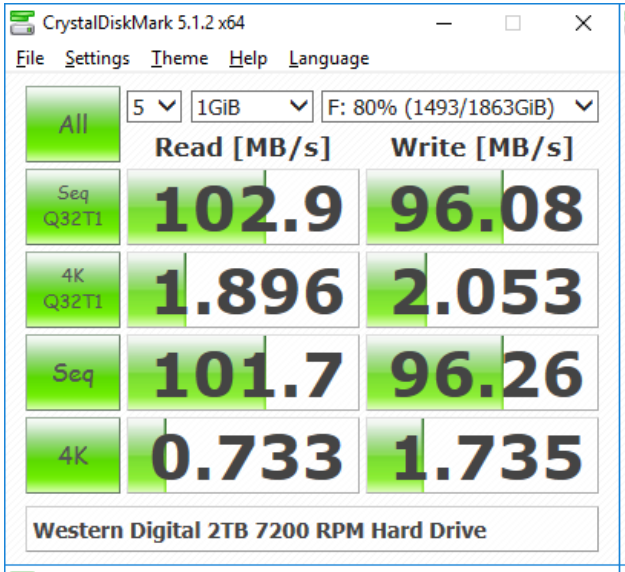
- NVMe M.2 1TB WD Black SN750 with the heatsink.
- SATA SSD, Crucial's MX500 in the 1TB flavor.
- well-known HDD WD's Black;
  - 6TB WD6003FZBX with a 256MB cache.

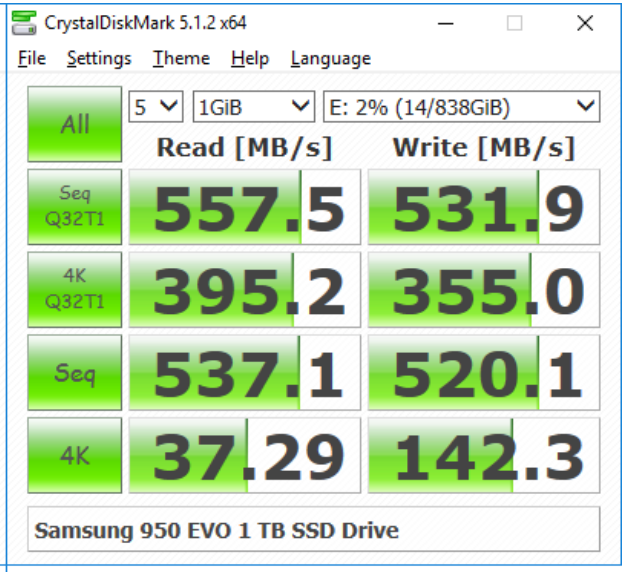
Average Random Write - 4KB QD1-4
iometer - IOPS - Higher is Better

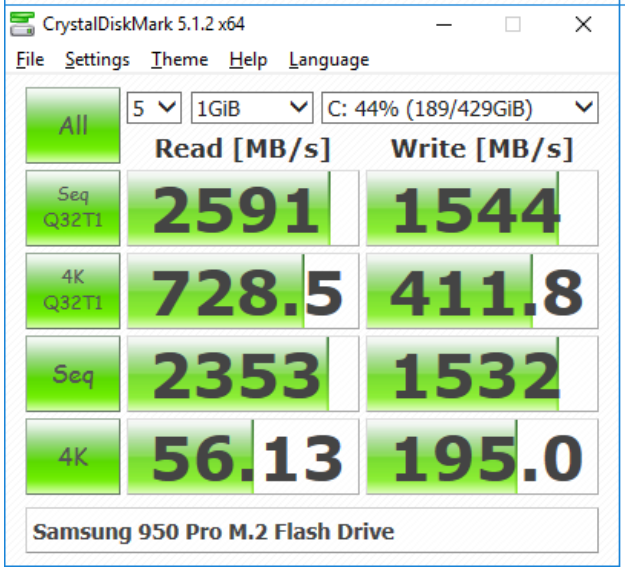
tom's HARDWARE



Comparison of SSD and HDD





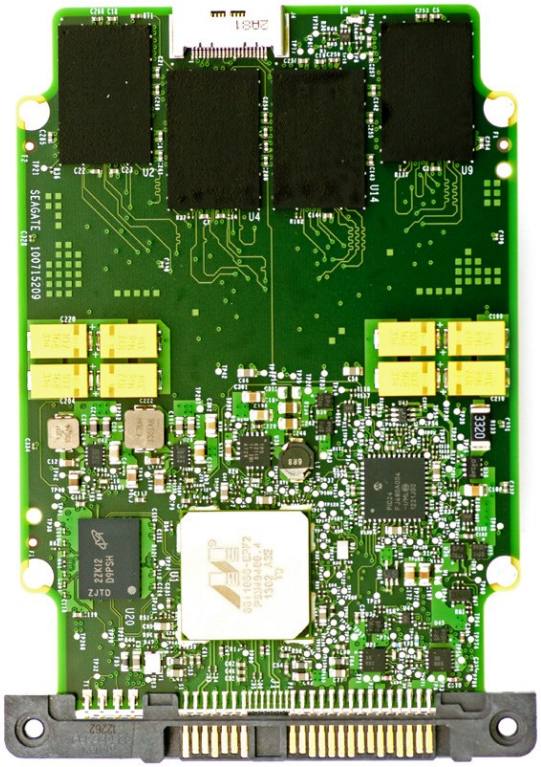


Performance Summary:

Hard Drive: 103 MB/sec read, 96 MB/sec write speed
SSD Drive: 558 MB/sec read, 532 MB/sec write speed
M.2 Drive: 2591 MB/sec read, 1544 MB/sec write speed

In Read Performance:
SSD is 5x Faster than HDD
M.2 is 5x Faster than SSD
M.2 is 25x Faster than HDD

Seagate 1200 SSD 400 GB



Seagate Savvio 15K.3 300 GB

Comparison of SSD and HDD - older

Year 2013	SSD Seagate 1200 SSD	HDD Seagate Savvio 15K.3
Sequential read	750 MB / s (128 KB)	176.5 MB / s
Sequential write	95 MB / s (128 KB)	176.5 MB / s
Random read	110,000 IOPS (4KB page)	543 IOPS (4KB sector)
Random write	40,000 IOPS (4KB page)	428 IOPS (4KB sector)
Average access time read / write	192 µs / 45 µwith	4.9 ms / 5.3 ms
MTBF (Mean Time Beetwen failure)	2,000,000 hours (0.44%)	2,000,000 hours (0.44%)
BER (Bit Error Ratio)	10^{-16}	10^{-16}
Consumption R/W / Idle	3.71 W / 2.72 W	7.92 W / 4.23 W
Price for GB	$ 3.65	$ 0.75

IOPS - Input/Output Operations Per Second

Comparison (selection) of HDD, SSHD, SSD drives for laptop

Laptop Storage Selection Criteria

	Speed	Capacity	Price	Reliability	Form Factor	Durability	Battery Life
HDD	★	★★★	★★★	★★★	★★	★★	★★
SSHD	★★	★★★	★★	★★★	★★	★★	★★
SSD	★★★	★	★	★★★	★★★	★★★	★★★

KEY: ★ = Good ★★ = Better ★★★ = Best

Source: www.seagate.com

