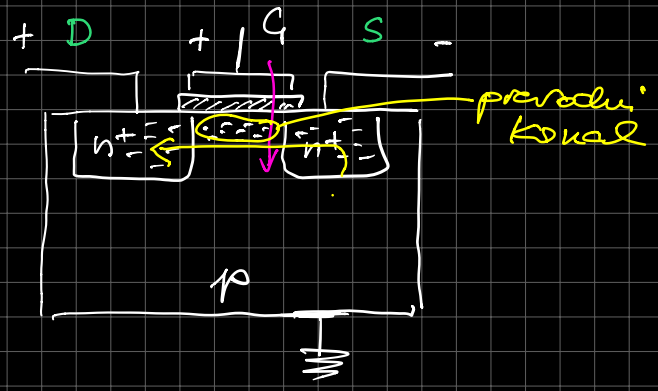
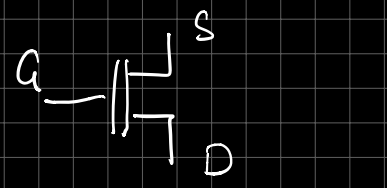
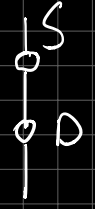
Ponovitev: CMOS T

n-kanalni T

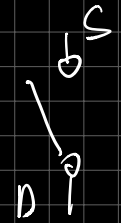




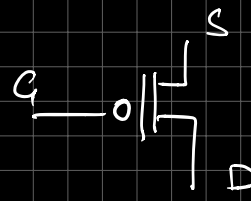
G = "1" :



G = "0" :



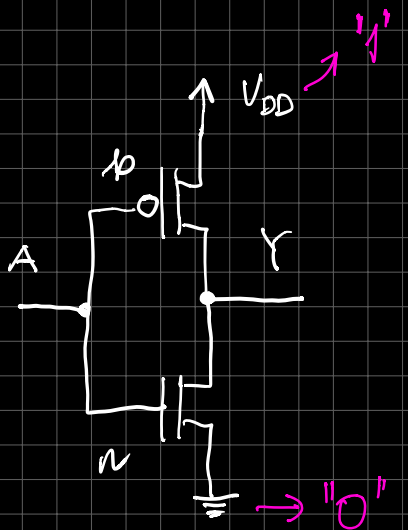
p-kanalni T



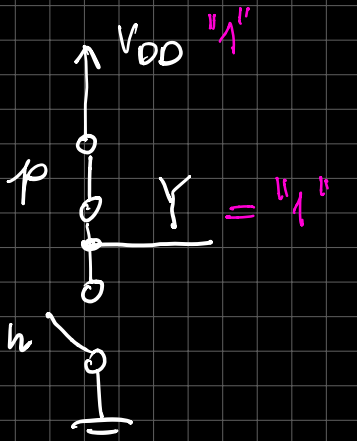
G = "0"

G = "1"

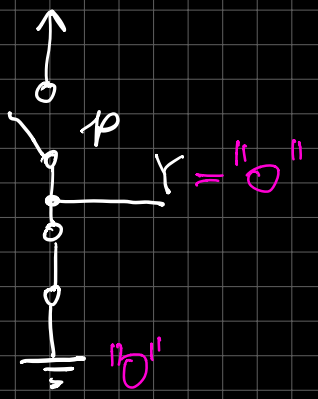
CMOS INVERTER



A="0": pT prevajata
nT ne prevajata



A = "1": pT ne prevajata
nT prevaja



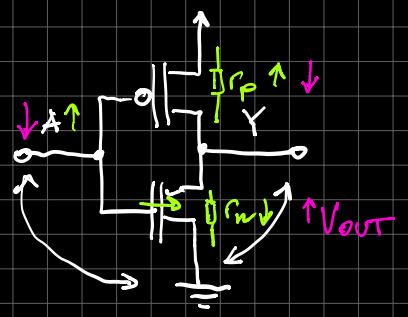
A	Y
0	1
1	0

} Inverter

Kako inverter preklaplja? ⇒ to mi najbolje prikaže t.i. PRENOSNA KARAKTERISTIKA

Prenosna karakteristika CMOS

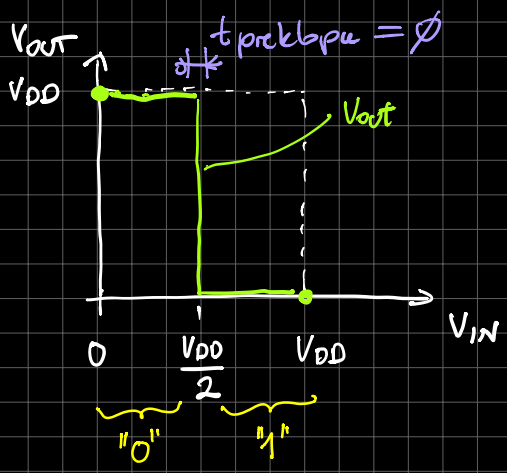
Inverter

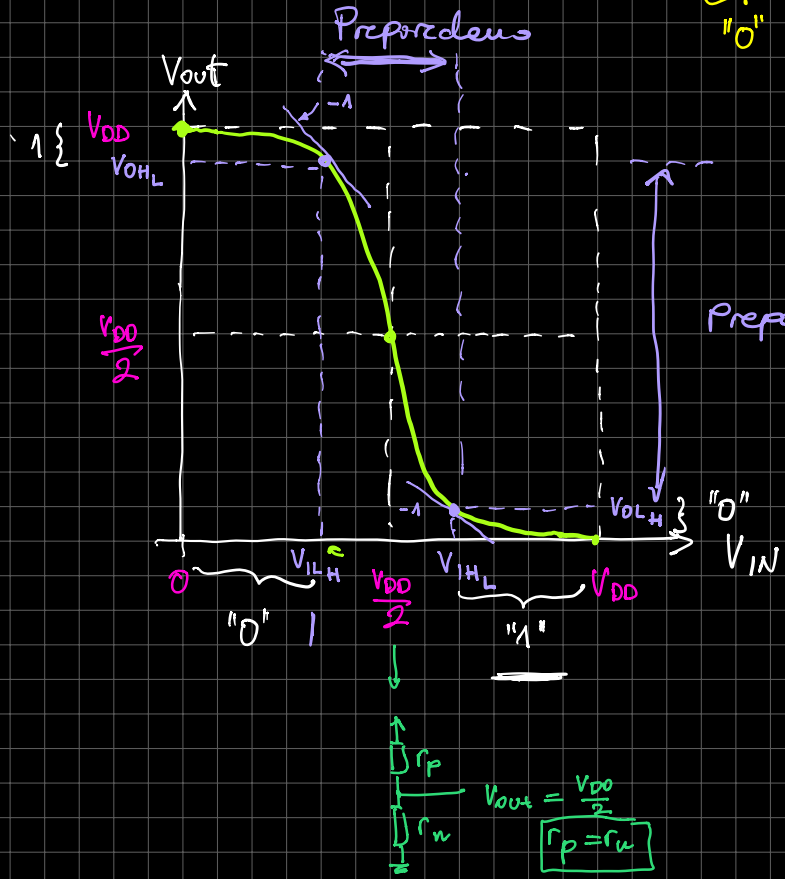


V_{IN}

če bo $V_{IN} = \frac{V_{DD}}{2} \Rightarrow r_p = r_n$

IDEALEN SVET:





V_{IL_H}: max vhodna napetost, ki še predstavlja logično 0

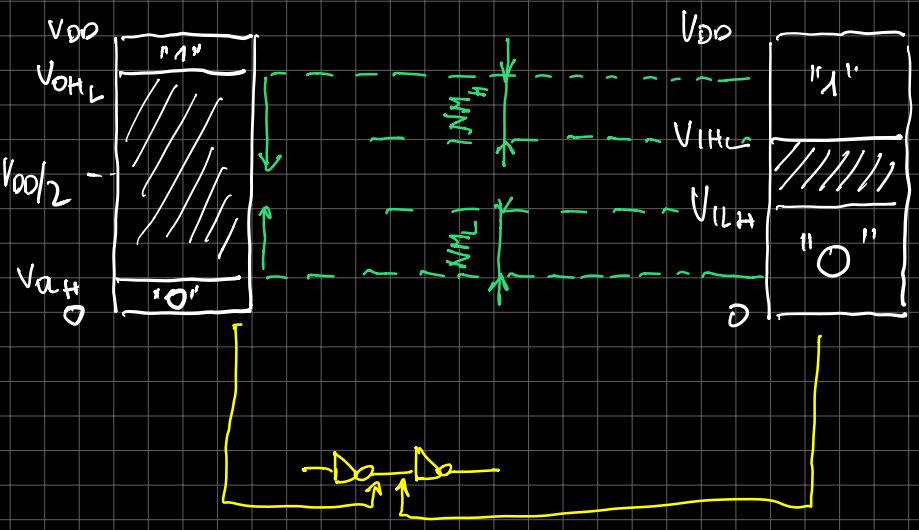
V_{OH_L}: min izhodna napetost, ki še predstavlja logično 1

V_{IH_L} : min vhodna napetost, ki še predstavlja log. 1

V_{OL_H} : max izhodna napetost, ki še predstavlja log. 0

↳ s temi vrednostmi so definirani t.i. logični nivoji

Logični nivoji na izhodu | Logični nivoji na vhodu

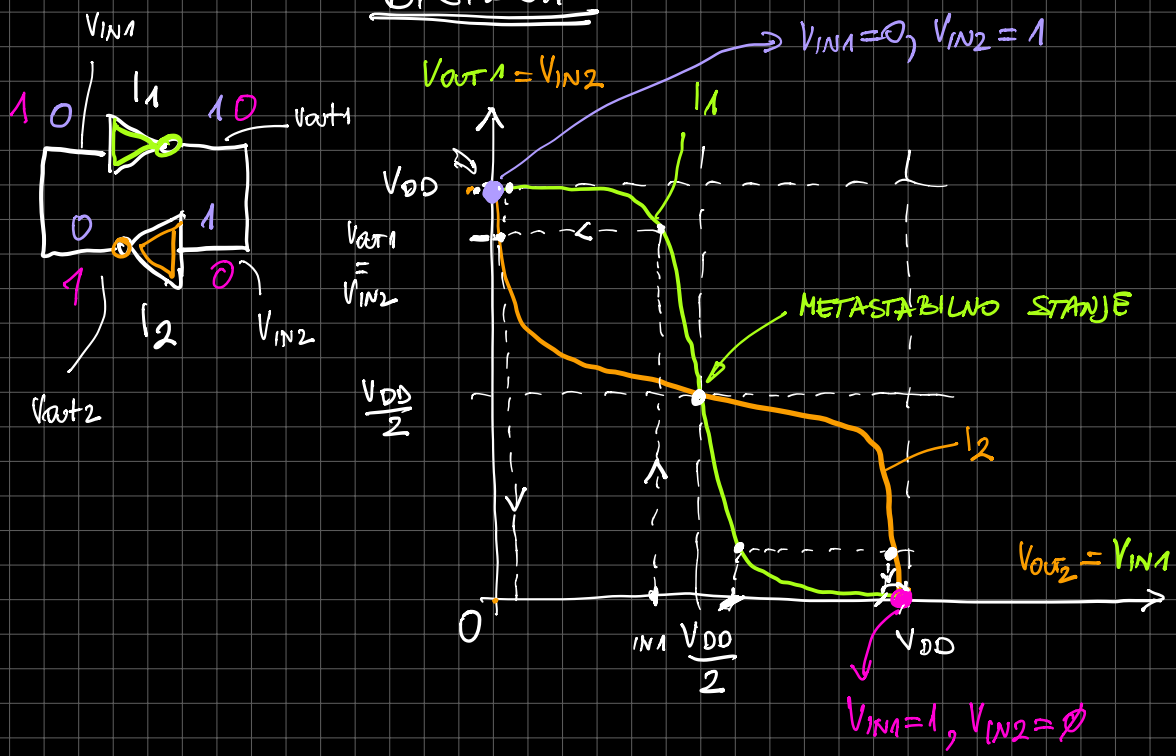


NM → noise margin (margina šuma)

$$NM_H = V_{OH_L} - V_{IH_L} \geq 0$$

$$NM_L = V_{IL_H} - V_{OL_H} \geq 0$$

Bistabil



↳ super kostroat bistabilo:

→ če je naum vhod zaradi šuma na I_1 premaknu prebitim $\frac{V_{DD}}{2}$, ga bo povratna vezava hitro pospešila v 0 in ujele bistabil v stabilno stanje

→ če se nam vhod zaradi šuma na I_1 od "1" preveč premakne proti $V_{DD}/2$ ga bo povratna vezava vrnilo v stabilno stanje

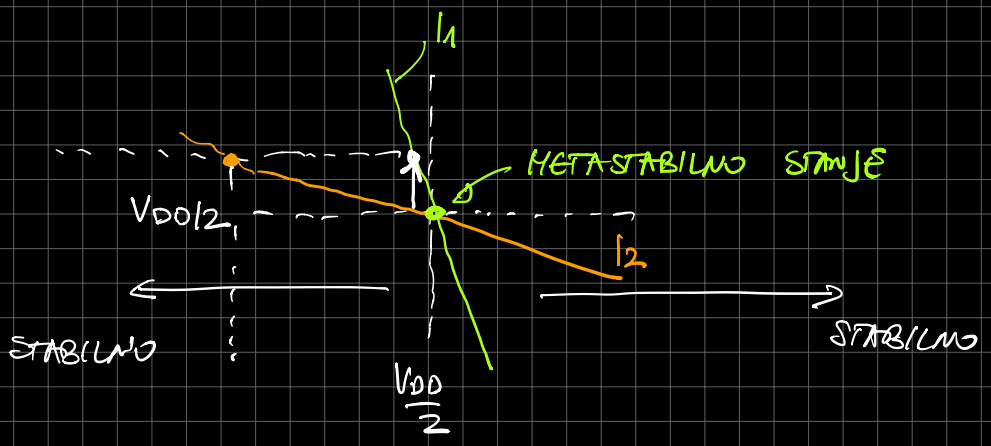
Kaj se zgodi, če je $V_{IN1} = V_{DD}/2 \rightarrow V_{OUT1} = V_{DD}/2$

↳ $V_{IN2} = V_{out1} = V_{DD}/2 \rightarrow V_{OUT2} = V_{DD}/2$

Novo, tretje, stabilno stanje!

META STABILNO STANJE

→ Kako stabilno je METASTABILNO stanje?



→ ni prav dolgo stabilno ⇒ to pomeni, da nas sporoči v eno od dveh stabilnih stanj ☺

SHIT: Čas je popolnoma naključen pojav

⇓

ne znam v katero stabilno stanje se bistabil sprosti iz METASTABILNEGA

Ne znam s 100% zanesljivostjo napovedati delovanja bistabila ☹

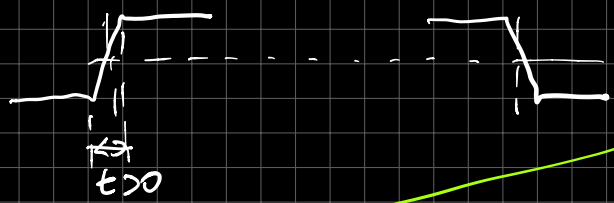
Če imam bistabil metastabilno stanje, potem bodite prepričani, da ga ima vsako dig. vezje

Kdo pri pomeri bi poten no vhod bistabila postal VDD/2

?

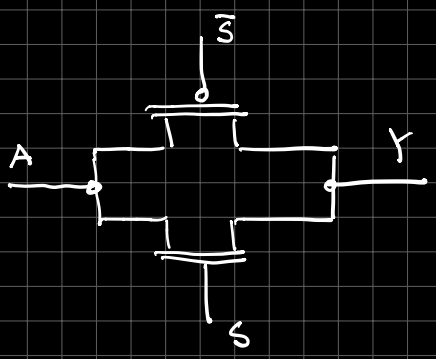
↳ skupno (vsaka) vprašanje

Problem je, da se vhodi spreminjajo => ZVEZNO!



Koji se vprašamo, bodo zaključili, da par. celice ne bodo "videle" VDD/2

TRANSMISSION GATE



a) Če je S=0:

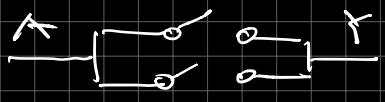
$G_n = 0$, $G_p = 1$

⇓

obu tranzistorja zaprta

⇓

nobeno stikalo ni sklenjeno

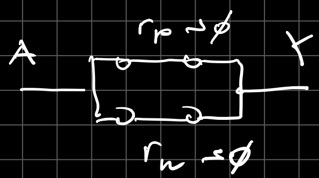


Y = Hi-Z (Z)

b) Če je $S = 1$:

$G_n = 1$, $G_p = 0$ $\Rightarrow$ prevajata oba tranzistorja

$\Downarrow$ obe stikali sklenjeni



$Y = A$

$\searrow$ $r = r_p \| r_n < r_p, r_n$

<u>Naslednjič</u>:

zapah D: dva INV + dva TG

flip-flop D: 4 INV + 4 TG

$\swarrow$ to bomo obdelali naslednjič

$\swarrow$ in potem spoznali, zakaj naj FF "gleda stran" od $\frac{V_{DD}}{2}$