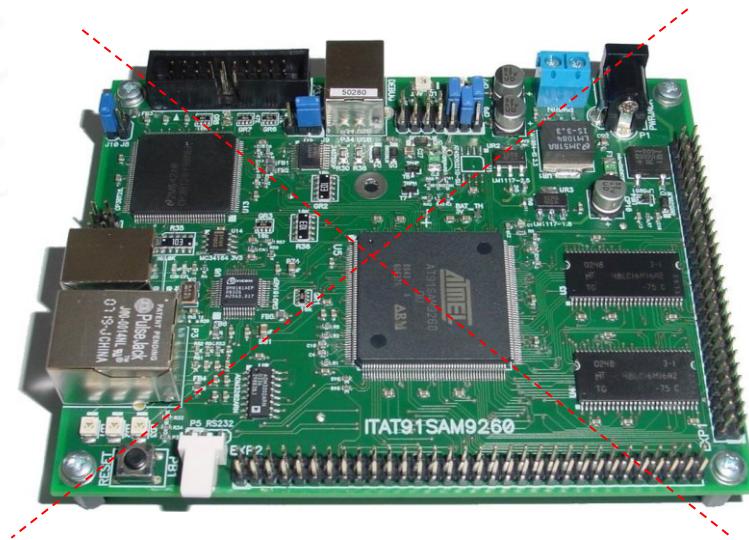


Computer architecture CA

Computer STM32H750-DK



- Računalnik FRI-SMS
 - Mikrokrmlnik AT91SAM9260 iz družine mikrokrmlnikov ARM9



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Instructors



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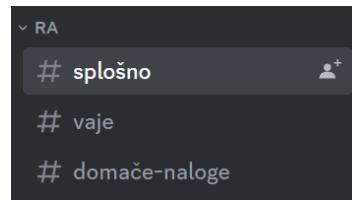


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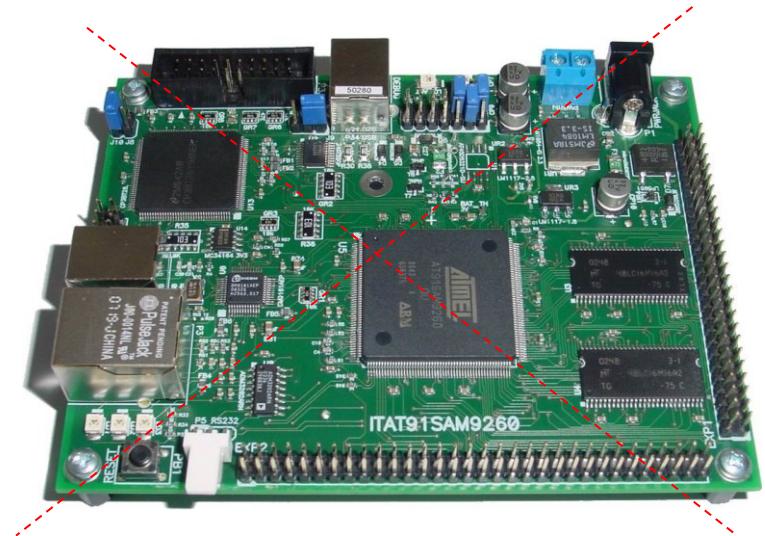
Computer architecture CA

Computer STM32H750-DK



- Računalnik FRI-SMS

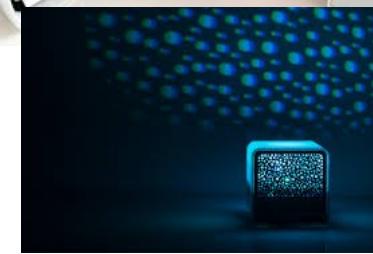
- Mikrokontroler AT91SAM9260 iz družine mikrokontrolnikov ARM9



LAB 1.1 General information

Laboratory exercises

- Learning the foundations of computer architecture from a practical view
- Understanding “How the computer works” by programming in ARM assembly language
- In-depth views:
 - computer operation
 - program execution
- Content upgrades: Computer Organization, Input/Output devices and other elective courses



Content of LAB work



- Basic knowledge needed from lectures (e.g. memory address, memory words, ...)
- Core: Programming in ARM assembly language
- Format:
 - lab exercises (2 hands-on exercises) + 1 homework assignment
- 3 intermediate exams (quizzes during lab sessions) - (november, december, january)
- Final exam preparations and exercises
- Alternative way: course seminar for advanced students – talk to instructor
- Video tutorials :
 - [Računalniška arhitektura \(RA\) \(sharepoint.com\)](#)

Evaluation – grading

- Lab marks represents **50% of the final mark** for the course. You need to have:
 - successfully evaluated **lab work** (presence, work)
 - successfully evaluated **homework assignment**,
 - three **intermediate evaluation exams** (80 + 100 + 120 points)
 - only condition: gather **at least 150 points (50%)**
 - no additional conditions on results of evaluation exam
- Final lab grade is valid only for the current academic year. You need to repeat lab work in new school year.

Web simulator cpulator

- <https://cpulator.01xz.net/?sys=arm>
- Base project for CA course:
 - <https://cpulator.01xz.net/?sys=arm&loadasm=share/sg8L1Nt.s>

The screenshot shows the cpulator web-based ARM debugger interface. The top navigation bar includes buttons for Stopped, Step Into (F2), Step Over (Ctrl-F2), Step Out (Shift-F2), Continue (F3), Stop (F4), Restart (Ctrl-R), Reload (Ctrl-Shift-L), File, and Help.

The main window is divided into several sections:

- Registers:** Shows the state of registers r0 to pc. The pc register is highlighted in red.
- Editor (Ctrl-E):** Displays the assembly code:

```
1 .text
2 .org 0x20
3 @spremenljivke
4 stev1: .word 0x40
5 stev2: .word 0x10
6 rez: .space 4
7
8 .align
9 .global _start
10 _start:
11
12 @program
13 adr r0, stev1
14 ldr r1, [r0]
15
16 adr r0, stev2
17 ldr r2, [r0]
18
19 add r3, r2, r1
20
21 adr r0, rez
22 str r3, [r0]
23
24 end: b end
```
- Memory (Ctrl-M):** Shows a memory dump from address 00000040 to 000001e0, where all bytes are filled with 'aa'.
- Messages:** Displays compilation and linking information:

```
Compiling...
Code and data loaded from ELF executable into memory. Total size is 80 bytes.
Assemble: arm-altera-eabi-as -mffloat-abi=soft -march=armv7-a -mcpu=cortex-a9 -mfpu=neon-fp16 --gdwarf2 -o work/asmhSiYoH.s.o work/asmhSiYoH.s
Link: arm-altera-eabi-ld --script build_arm.ld -e _start -u _start -o work/asmhSiYoH.elf work/asmhSiYoH.s
Compile succeeded.
```

Computer architecture CA

Computer STM32H750-DK



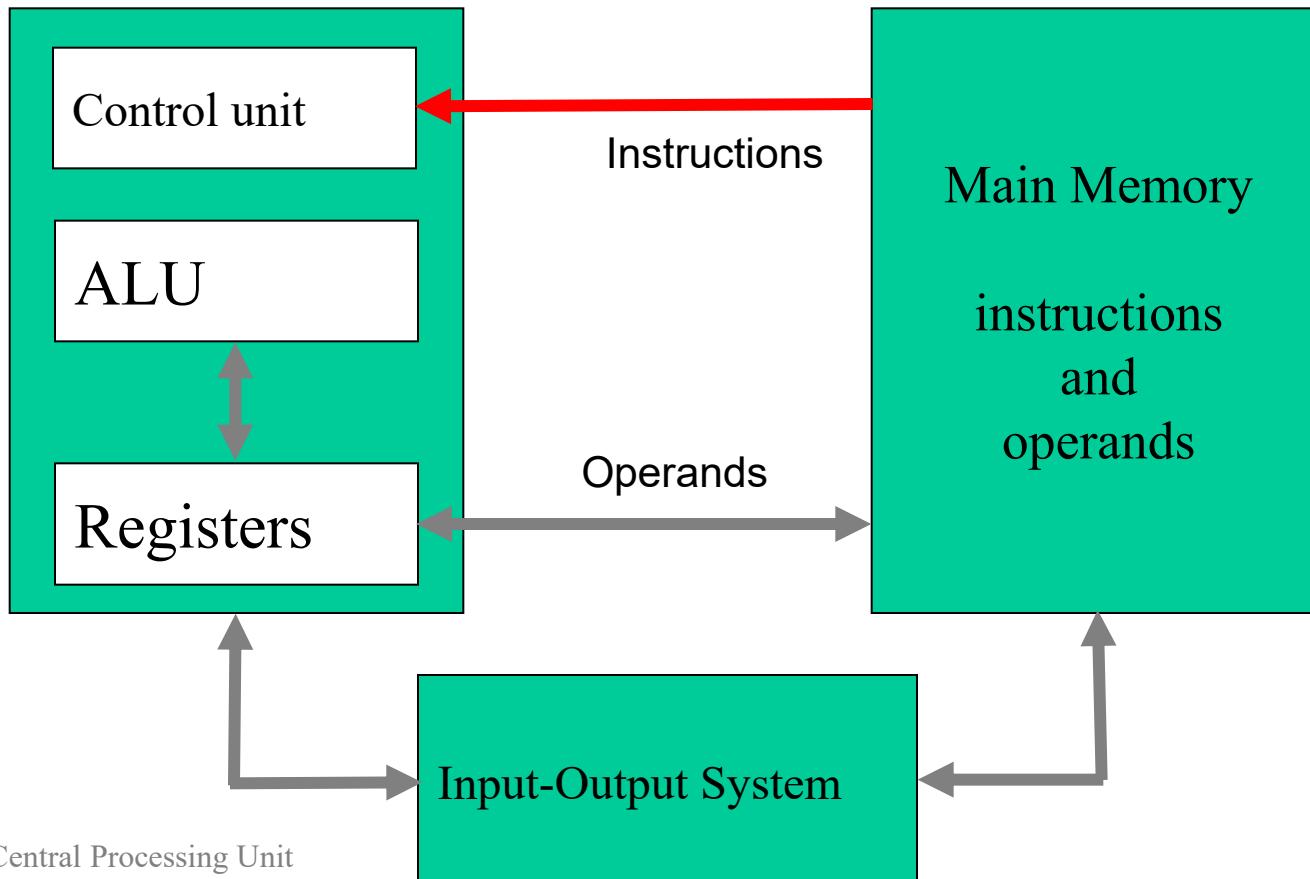
- Računalnik FRI-SMS
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LAB 1.2 Von Neumann model (VN)

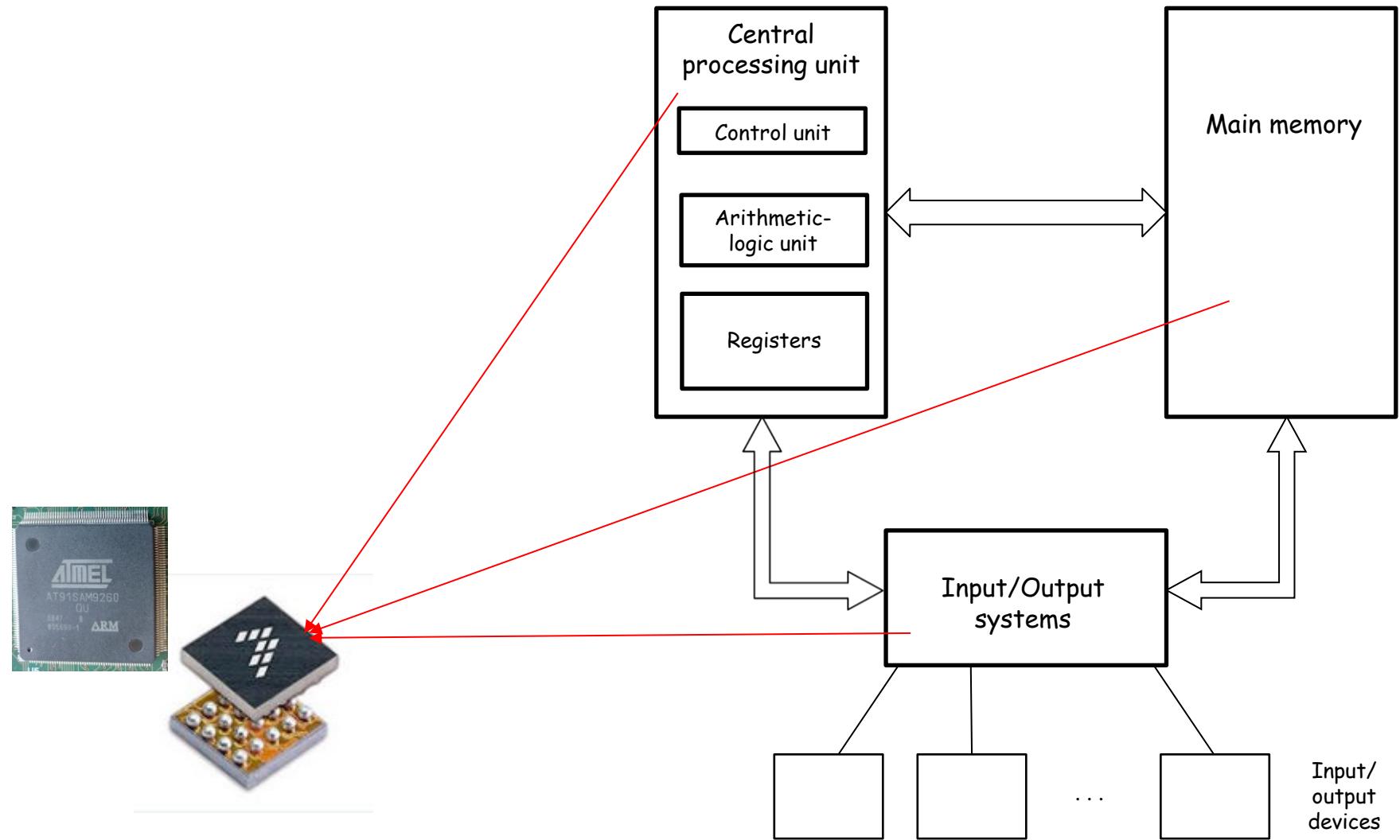
Von Neumann Computer Model

CPU



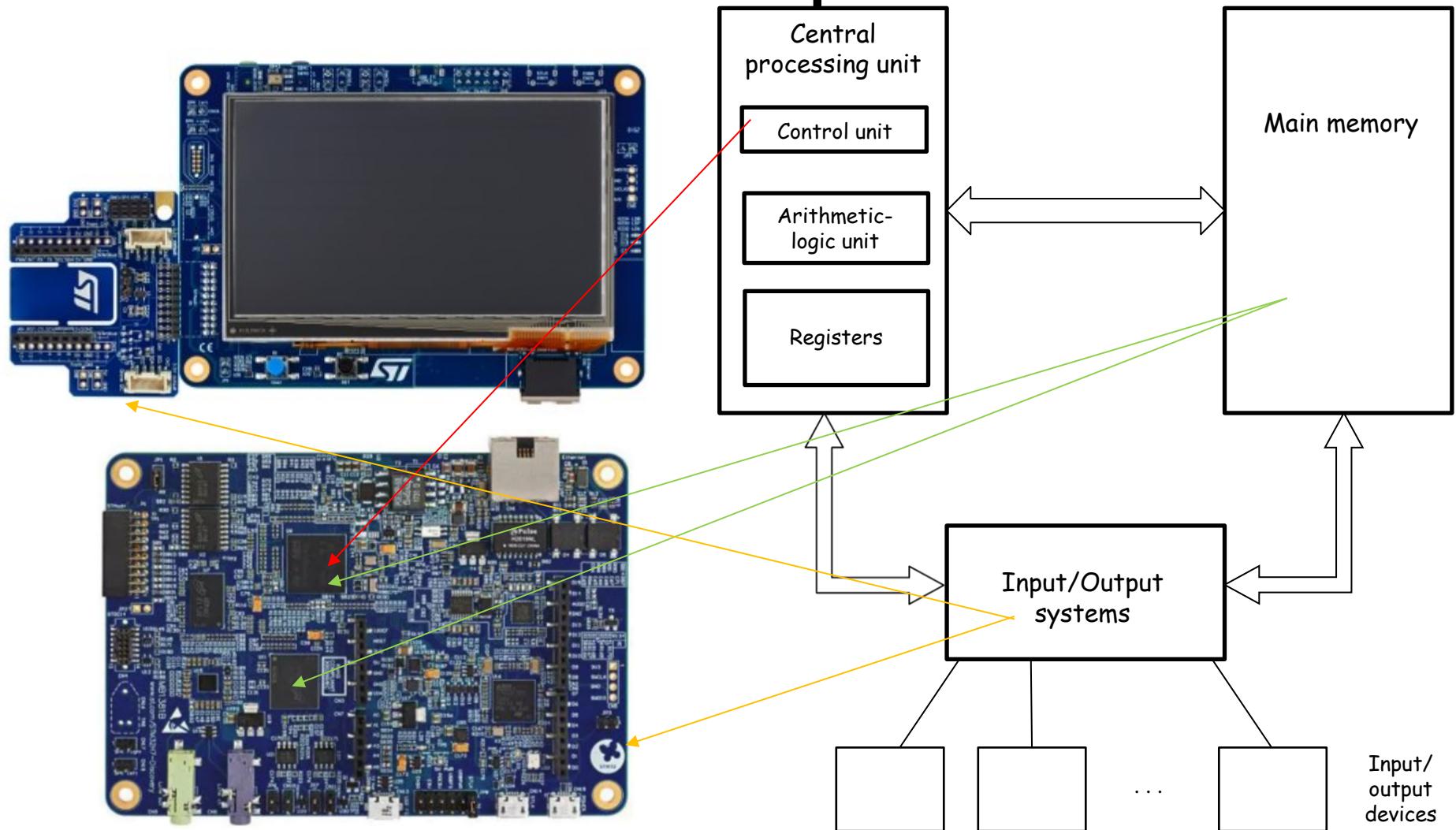
CPU – Central Processing Unit
ALU – Arithmetic Logic Unit

The basic computer model



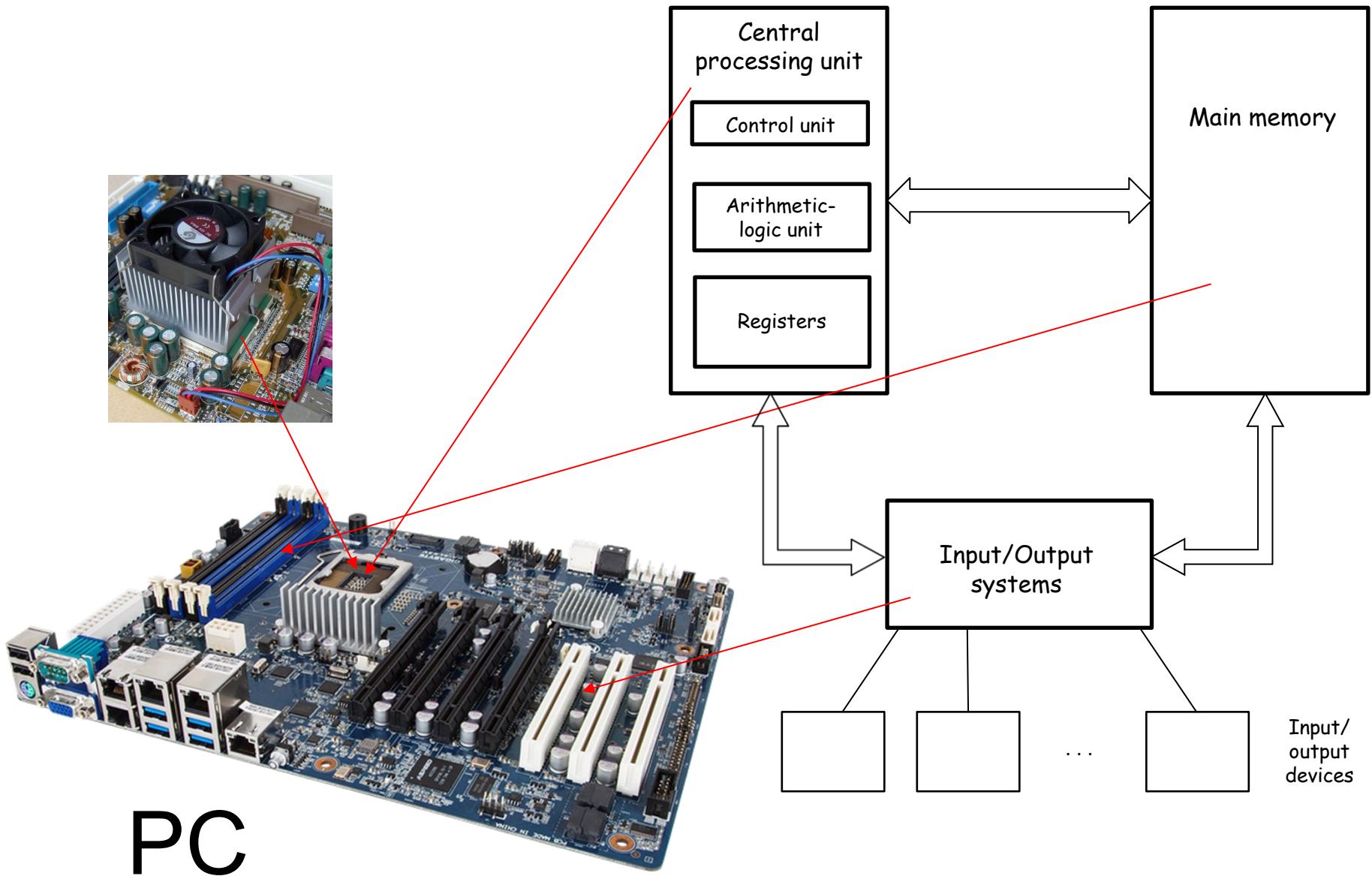
MicroControllers

The basic computer model



STM32H750-DK

The basic computer model

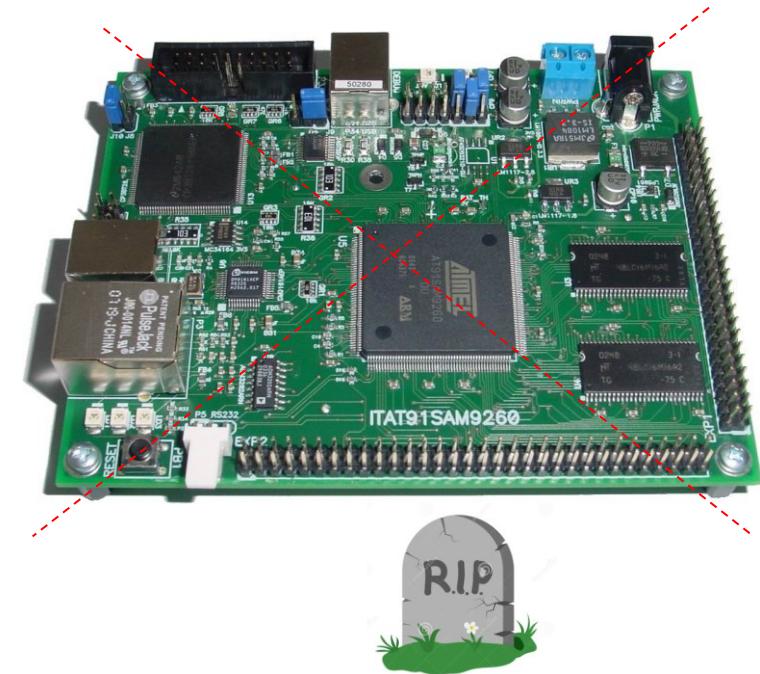


Computer architecture CA

Computer STM32H750-DK

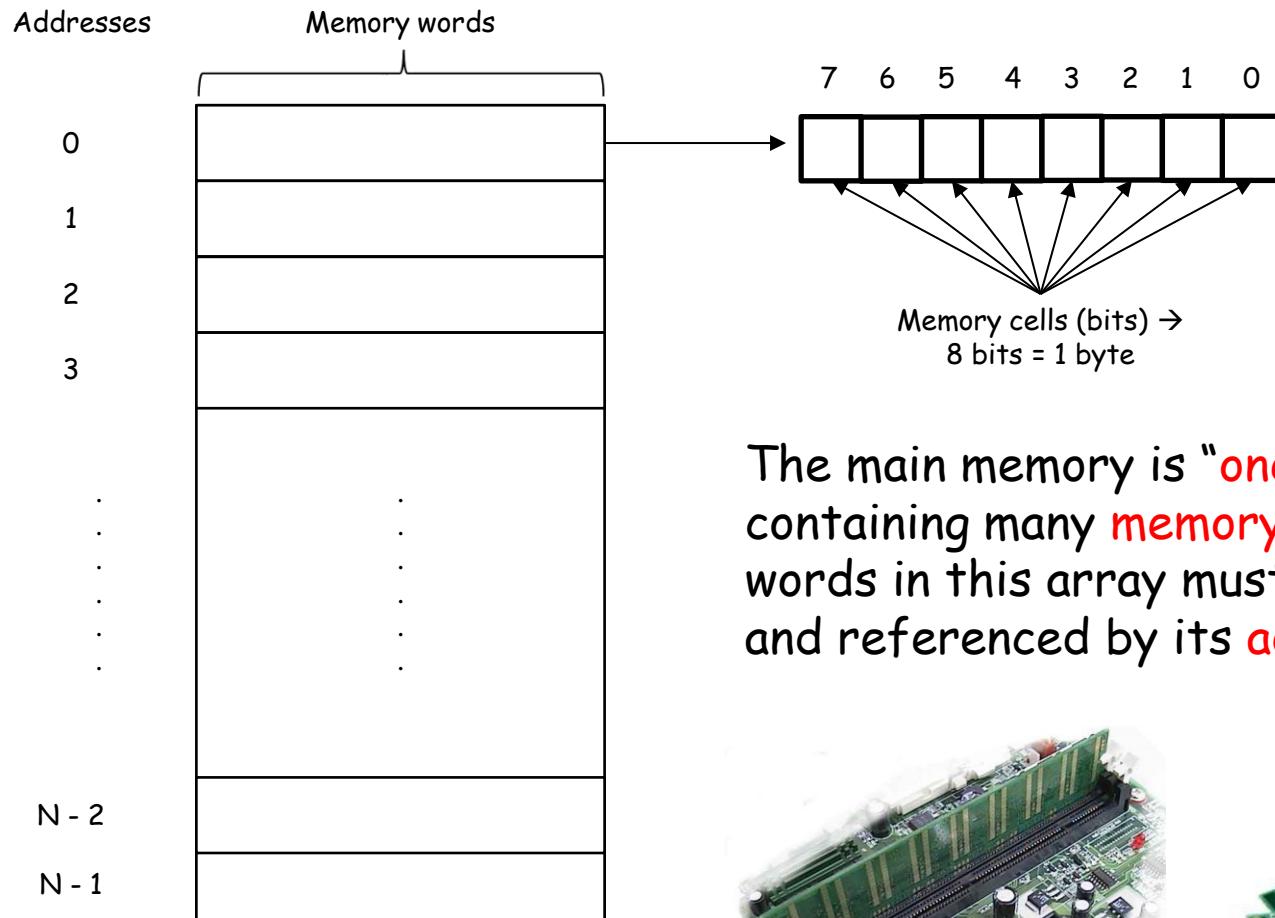


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LAB 1.3 Memory

What is memory ?



The main memory is “one dimensional array” containing many **memory words**. Each memory words in this array must be **uniquely** identified and referenced by its **address**!



Main Memory in von Neumann Computer

Memory Address		Memory words
Binary (length 16 bits)	Decimal	
0000 0000 0000 0000	0	
0000 0000 0000 0001	1	
0000 0000 0000 0010	2	
0000 0000 0000 0011	3	
0000 0000 0000 0100	4	
0000 0000 0000 0101	5	
.....		:

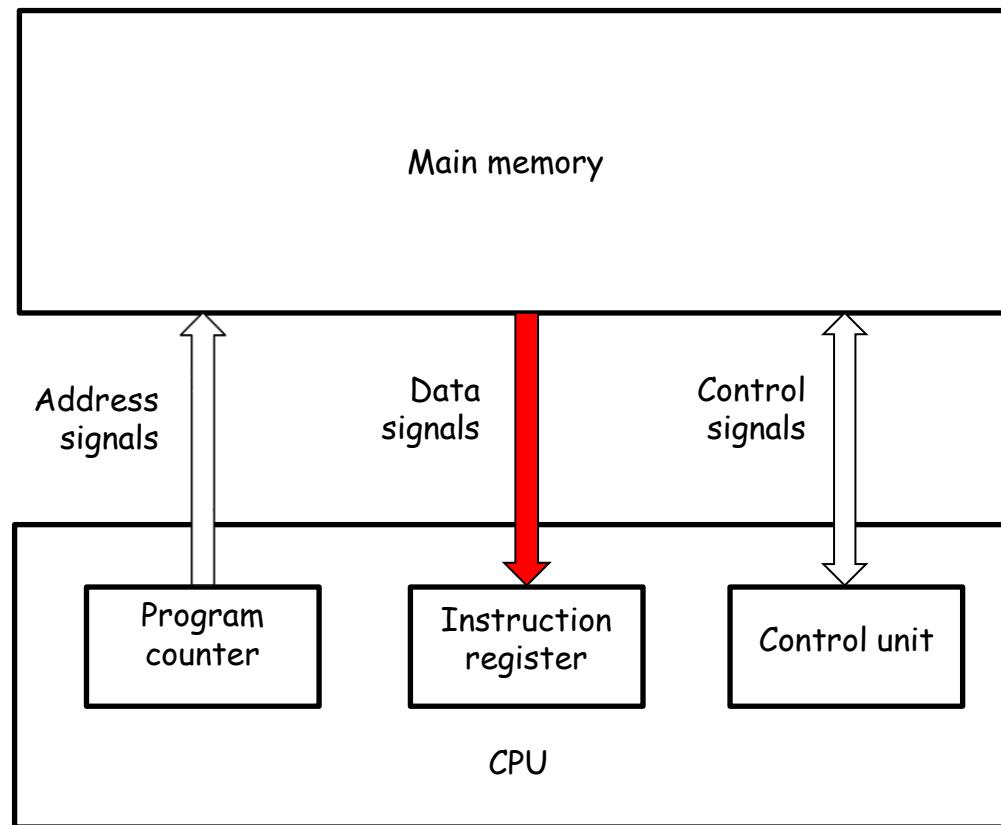


The diagram illustrates the mapping of memory addresses to memory words. On the left, a table shows memory addresses in binary (16 bits) and decimal. To the right, a vertical stack of boxes represents memory words. An arrow points from the first memory word box to a larger 16-bit box. This 16-bit box is divided into two 8-bit sections: the top section is labeled 'MSB' and the bottom section is labeled 'LSB'. The entire 16-bit box is labeled '8-bit memory word'.

Memory Address				
Binary (length 16 bits)	Hexadecimal	Decimal	Memory words	
0000 0000 0000 0000	0000	0		
0000 0000 0000 0001	0001	1		
0000 0000 0000 0010	0002	2		
0000 0000 0000 0011	0003	3		
0000 0000 0000 0100	0004	4		
0000 0000 0000 0101	0005	5		
.....	
.....	
1111 1111 1111 1011	FFFFB	65531		
1111 1111 1111 1100	FFFC	65532		
1111 1111 1111 1101	FFFD	65533		
1111 1111 1111 1110	FFFE	65534		
1111 1111 1111 1111	FFFF	65535		

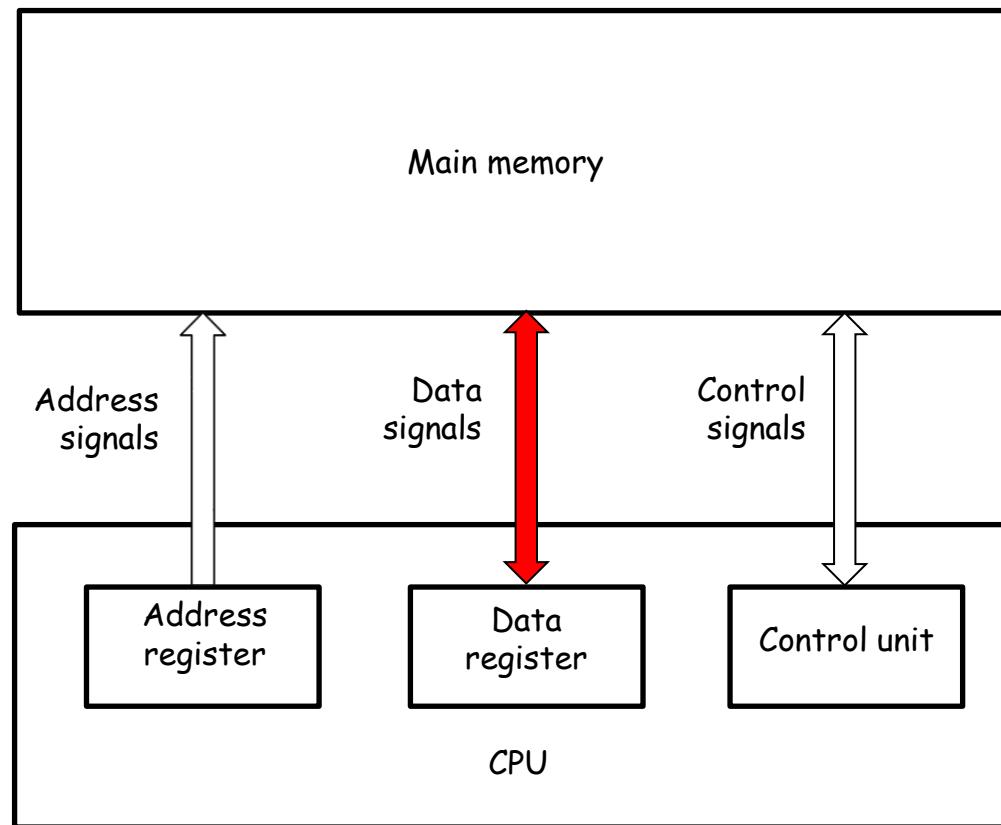
How does CPU access the main memory?

Example for accessing instructions:



How does CPU access the main memory?

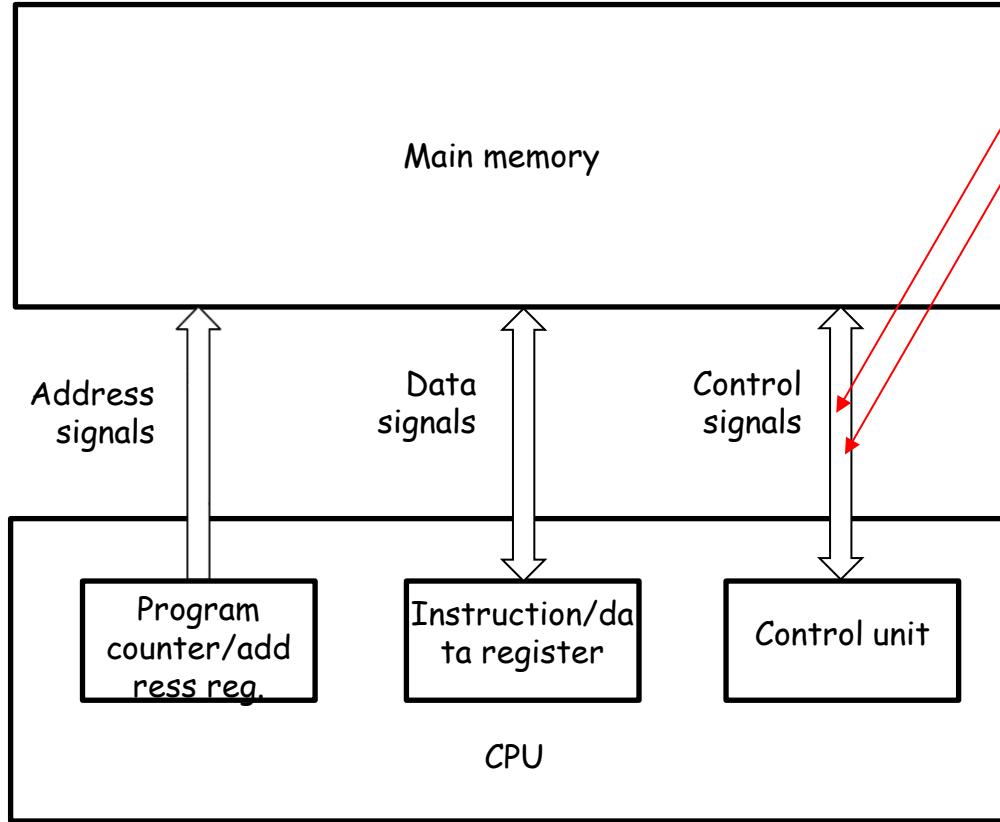
Examples for accessing operands:



Interconnection CPU <-> main memory

Bus = a group of related lines
(Address, Data, Control buses)

Line = physical connection
Signal = content transferred over the line (1bit)

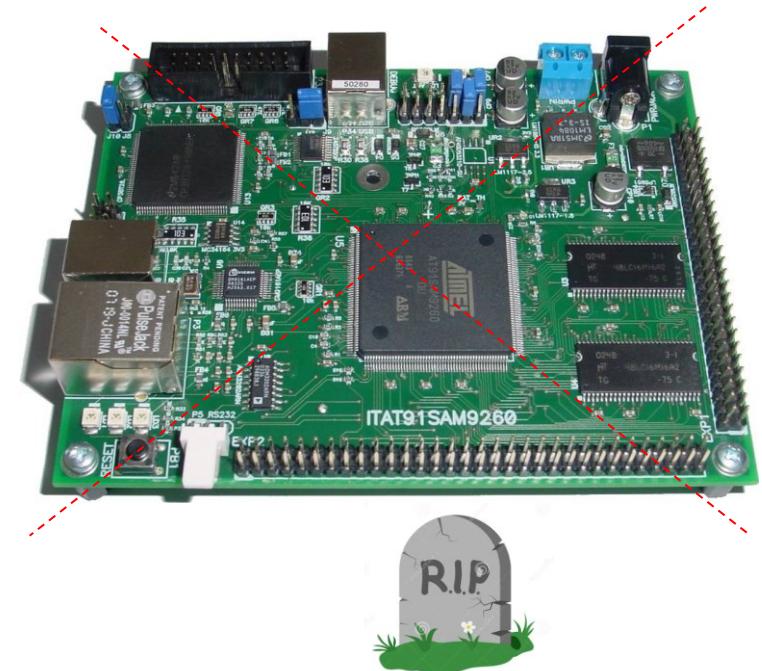


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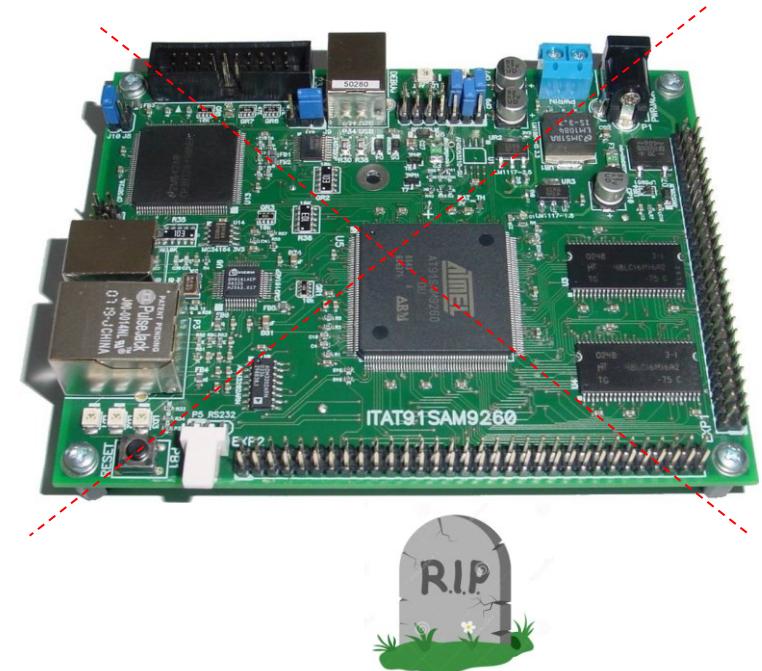
LAB 1.4 Quick intro to numeral systems

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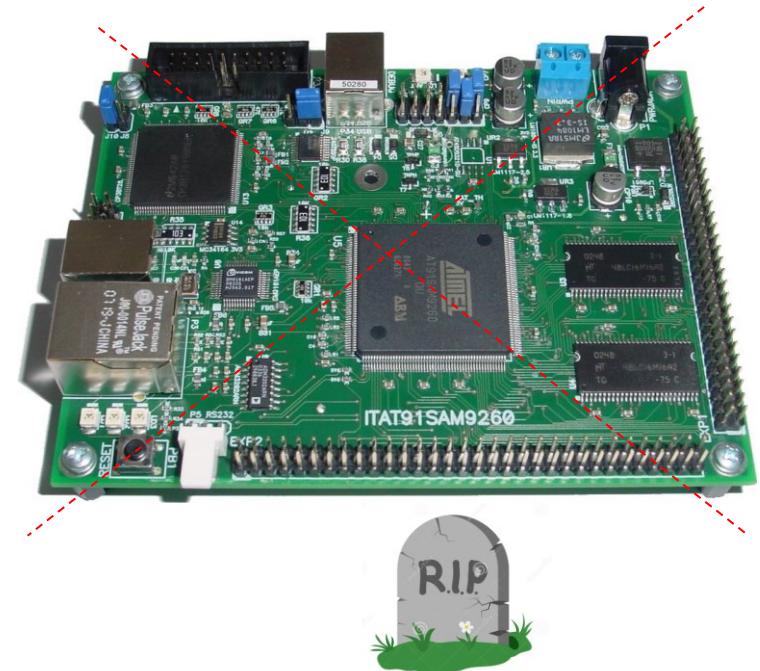
LAB 1.5 Big and Little Endian rules

Computer architecture CA

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LAB 1.6 Addition – human, python,
assembler cases

Human (case: $64 + 16 = 80$)

$$64 + 16 = ?$$

A handwritten addition problem is shown. The numbers 64 and 16 are written in black ink. A red question mark is placed between them. To the right, a red horizontal line separates the sum from the numbers. Above the line, the number 64 is written in red. Below the line, the number 16 is written in red, preceded by a plus sign. To the right of the line, the number 80 is written in red. A red curved arrow points from the question mark to the number 80.

$$\begin{array}{r} 64 \\ + 16 \\ \hline 80 \end{array}$$

Python (case: REZ = STEV1 + STEV2)

Adding two variables in Python.

<http://goo.gl/YXQ5qN>

Python 2.7

```
1 STEV1=0x40
2 STEV2=0x10
3 REZ = STEV1 + STEV2
→ 4 print (" STEV1 = " + hex(STEV1) + "\n+STEV2 = " + hex(STE
```

Frames

Global frame

STEV1 64

STEV2 16

REZ 80

Objects

Print output (drag lower right corner to resize)

STEV1 = 0x40

+STEV2 = 0x10

REZ = 0x50

WinIDEA (case: rez = stev1 + stev2)

Evaluate the sum of two variables in ARM assembler.

Use prepared project from e-classroom)

Variables values are stored in the main memory. We perform a simple arithmetic addition with the following instructions:

Assembly language	Instruction description	Machine language
adr r0, stev1	R0 \leftarrow Addr. of stev1	0xE24F0014
ldr r1, [r0]	R1 \leftarrow M[R0]	0xE5901000
adr r0, stev2	R0 \leftarrow Addr. of stev2	0xE24F0018
ldr r2, [r0]	R2 \leftarrow M[R0]	0xE5902000
add r3, r2, r1	R3 \leftarrow R1 + R2	0xE0823001
adr r0, rez	R0 \leftarrow Addr. of rez	0xE24F0020
str r3, [r0]	M[R0] \leftarrow R3	0xE5803000



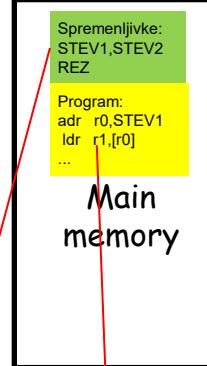
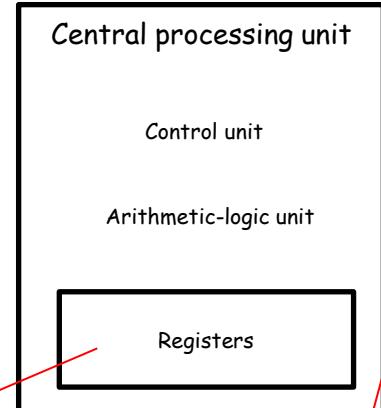
Execute instructions step-by-step and observe the register's values and the variable's values inside the main memory.

Practical example : Sum of 2 numbers

<https://cpulator.01xz.net/?sys=arm&loadasm=share/s8zU3xx.s>

Assembly language	Instruction description	Machine language
adr r0, stev1	R0 \leftarrow Addr. of stev1	0xE24F0014
ldr r1, [r0]	R1 \leftarrow M[R0]	0xE5901000
adr r0, stev2	R0 \leftarrow Addr. of stev2	0xE24F0018
ldr r2, [r0]	R2 \leftarrow M[R0]	0xE5902000
add r3, r2, r1	R3 \leftarrow R1 + R2	0xE0823001
adr r0, rez	R0 \leftarrow Addr. of rez	0xE24F0020
str r3, [r0]	M[R0] \leftarrow R3	0xE5803000

Assembler
(compiler)



Stopped

Step Into F2 Step Over Ctrl-F2 Step Out Shift-F2 Continue F3 Stop F4 Restart Ctrl-R Reload Ctrl-Shift-L File Help

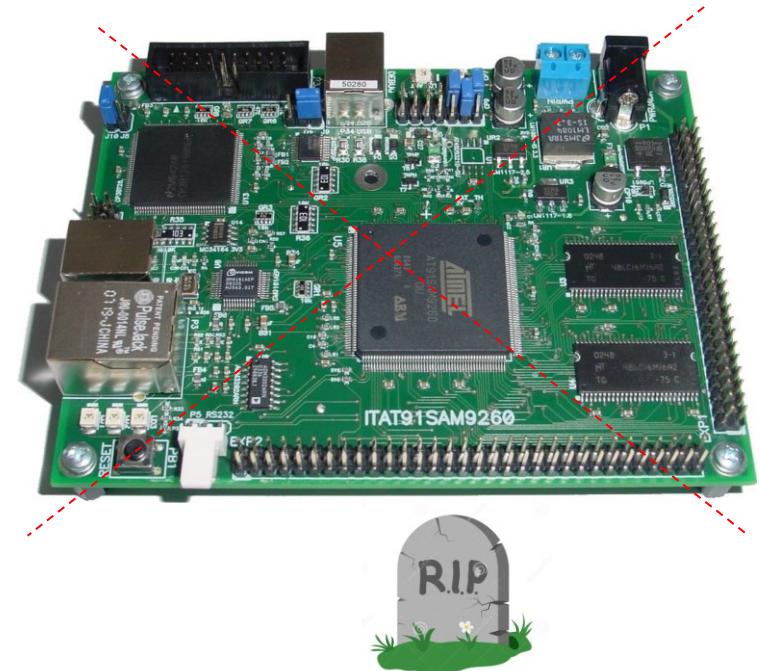
Registers			Disassembly (Ctrl-D)			Memory (Ctrl-M)																																																																																																											
Refresh			Go to address, label, or register: 00000000 <table border="1"> <thead> <tr> <th>Address</th> <th>Opcode</th> <th>Disassembly</th> </tr> </thead> <tbody> <tr> <td>00000020</td> <td>00000010</td> <td>STEV1: andeq r0, r0, r0,</td> </tr> <tr> <td>00000024</td> <td>00000040</td> <td>STEV2: andeq r0, r0, r0,</td> </tr> <tr> <td>00000028</td> <td>00000000</td> <td>REZ: andeq r0, r0, r0</td> </tr> <tr> <td>9</td> <td>.align</td> <td></td> </tr> <tr> <td>11</td> <td>.global _start</td> <td></td> </tr> <tr> <td>12</td> <td>_start:</td> <td></td> </tr> <tr> <td>14</td> <td>adr r0,STEV1</td> <td></td> </tr> <tr> <td></td> <td></td> <td>_start:</td> </tr> <tr> <td>0000002c</td> <td>e24f0014</td> <td>adr r0, 0x20 (C)</td> </tr> <tr> <td>00000030</td> <td>e5901000</td> <td>15 ldr r1, [r0]</td> </tr> <tr> <td></td> <td></td> <td>17 adr r0,STEV2</td> </tr> <tr> <td>00000034</td> <td>e24f0018</td> <td>18 add r0, 0x24 (C)</td> </tr> <tr> <td>00000038</td> <td>e5902000</td> <td>20 ldr r2, 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LAB 1.7 Notes – empty templates

Python (case: REZ = STEV1 + STEV2)

Frames

Objects

Global frame

STEV1 | 64

STEV2 | 16

REZ | 80

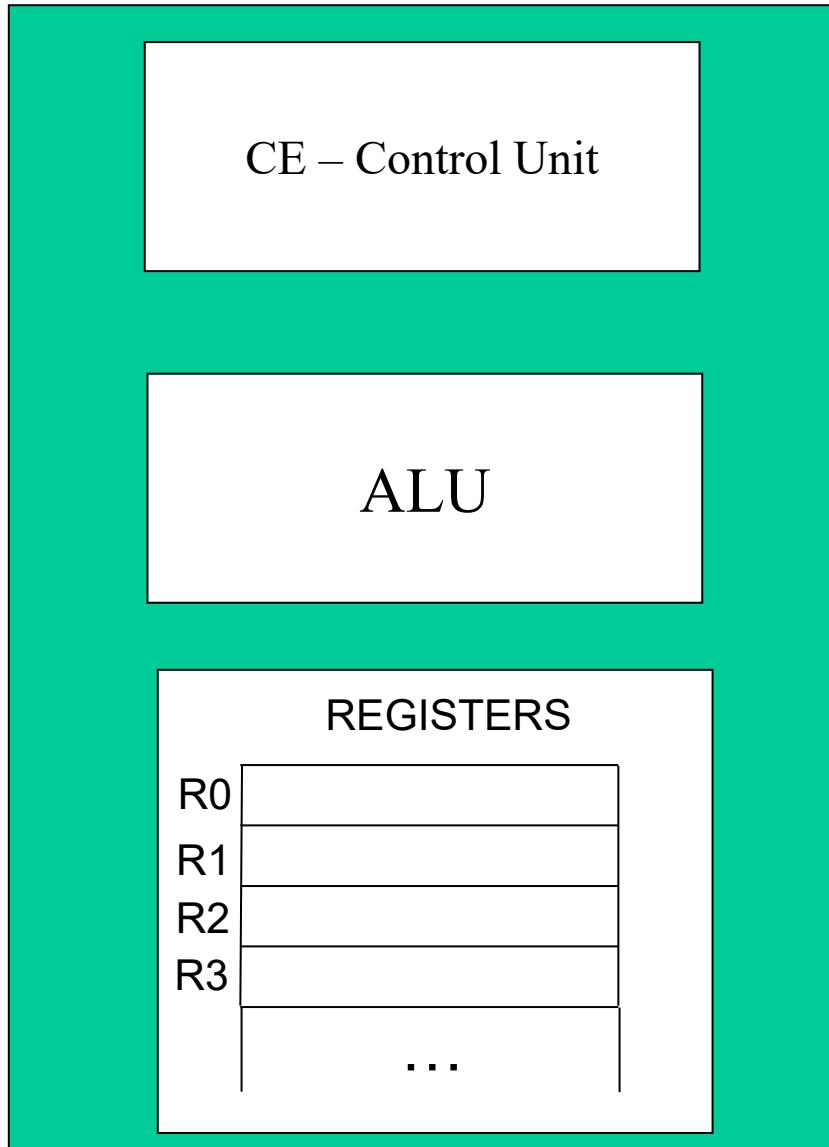
Python 2.7

```
1 STEV1=0x40
2 STEV2=0x10
3 REZ = STEV1 + STEV2
→ 4 print (" STEV1 = " + hex(STEV1) + "\n+STEV2 = " + hex(STE
```

<http://goo.gl/YXQ5qN>

Case: adding two numbers

CPU



Memory

Address	Memory words (locations)	Label Content
0x00 = 0		
0x01 = 1		
0x02 = 2		
...		
0x20 = 0		STEV1
0x24 = 4		STEV2
0x28 = 8		REZ
0x2C = 12		1. instruction ADR R0,STEV1

INSTRUCTIONS

	Machine Instr.	Assembly Instr.	Description	Comment
1.	0xE24F0014	adr r0, stev1	$R0 \leftarrow \text{Addr. of stev1}$	
2.	0xE5901000	ldr r1, [r0]	$R1 \leftarrow M[R0]$	
3.	0xE24F0018	adr r0, stev2	$R0 \leftarrow \text{Addr. of stev2}$	
4.	0xE5902000	ldr r2, [r0]	$R2 \leftarrow M[R0]$	
5.	0xE0823001	add r3, r2, r1	$R3 \leftarrow R1 + R2$	
6.	0xE24F0020	adr r0, rez	$R0 \leftarrow \text{Addr. of rez}$	
7.	0xE5803000	str r3, [r0]	$M[R0] \leftarrow R3$	

Pravilo tankega in debelega konca / Big vs. Little Endian

MSB LSB

0 x AA BB CC DD

Debeli konec
Big Endian



Tanki konec
Little Endian

