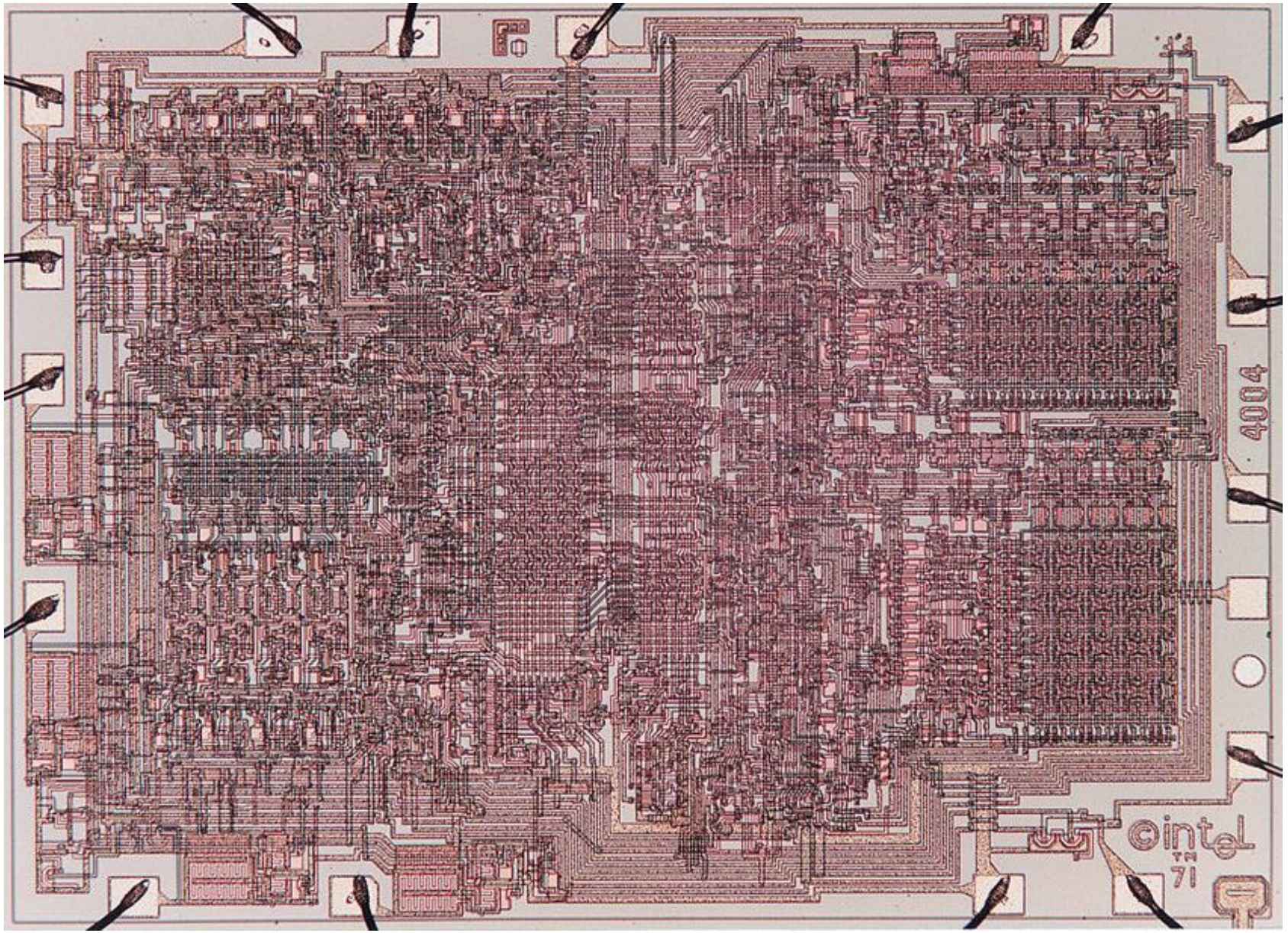
02
Tehnologija ASIC/FPGA, načrtovalski cikel

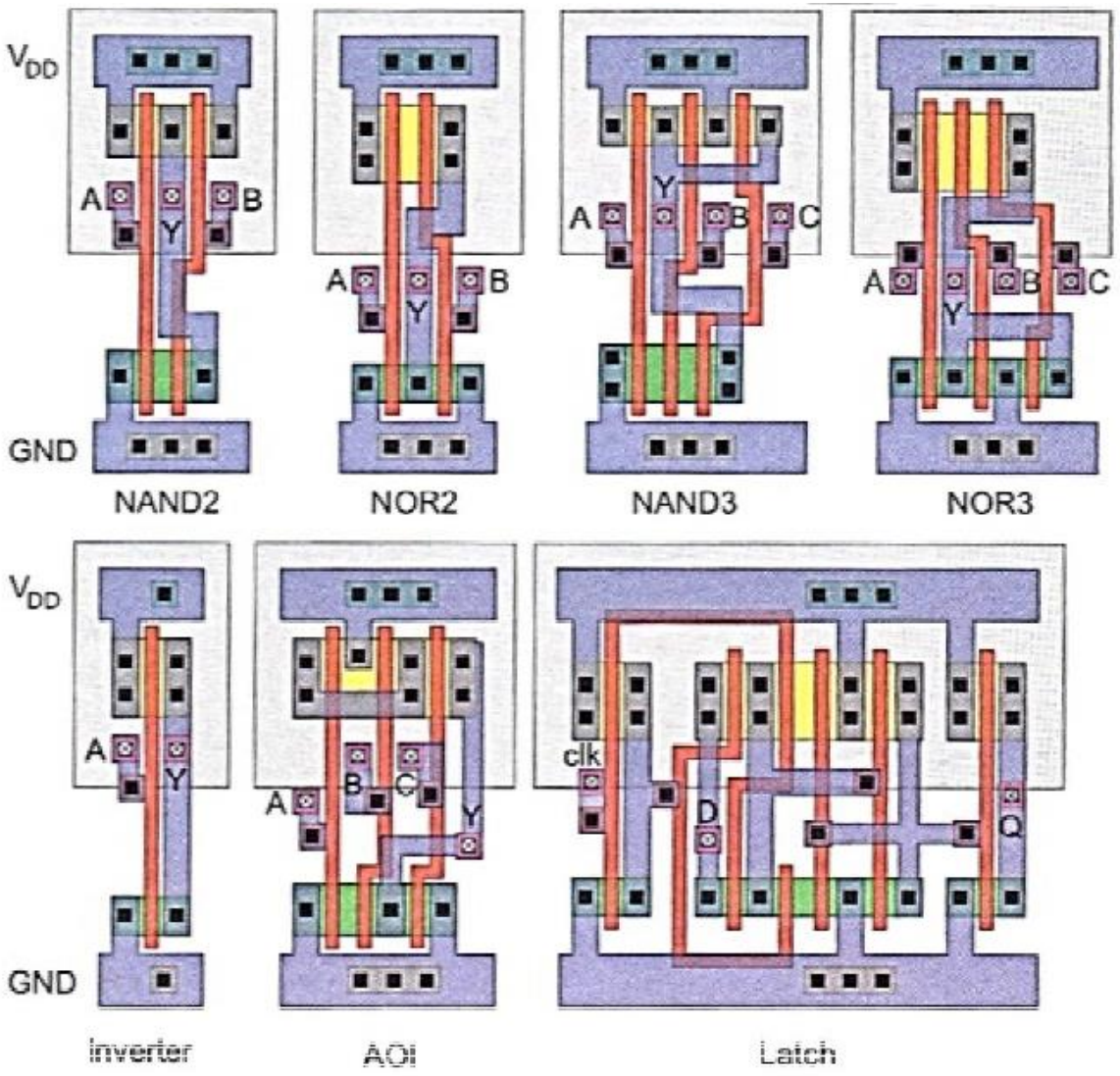
Digitalno načrtovanje

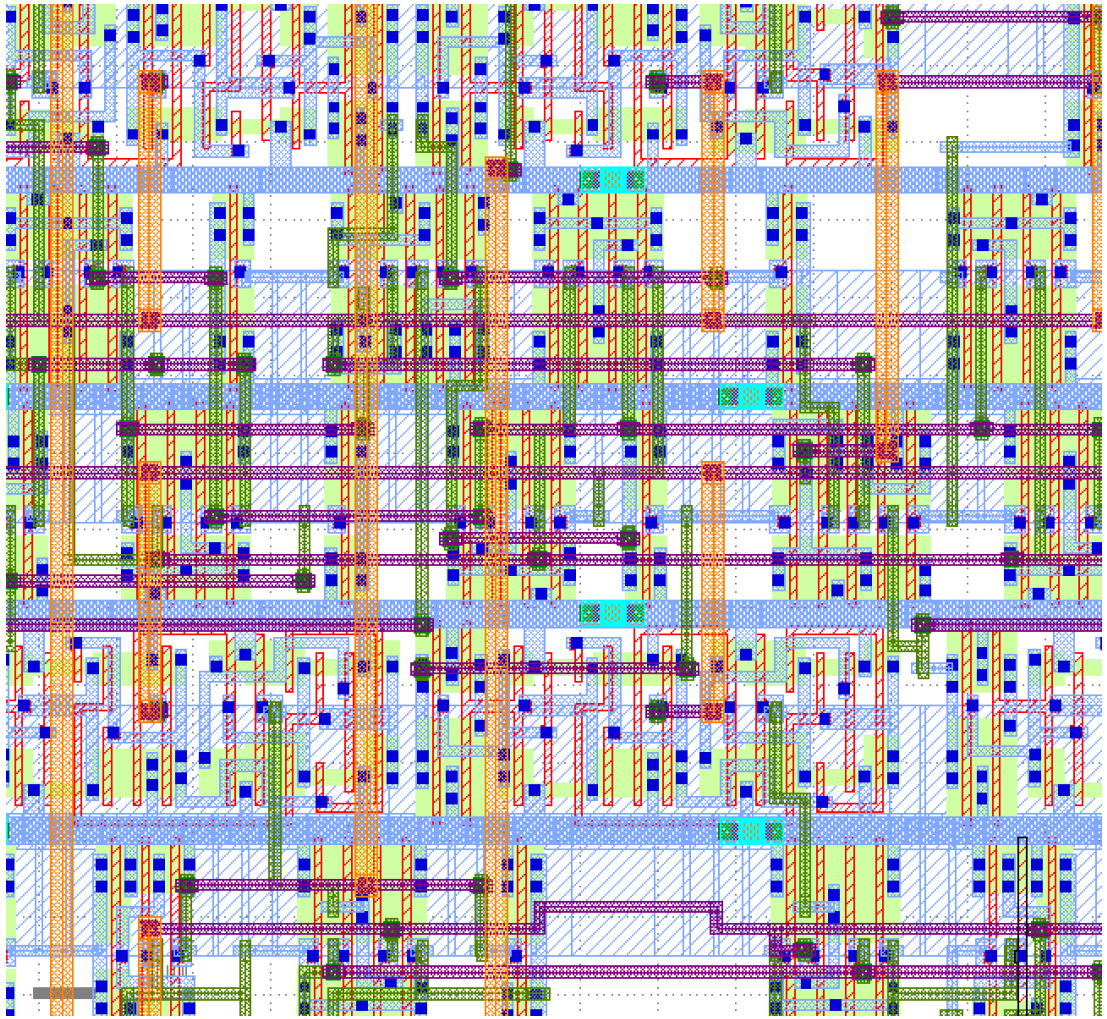
Patricio Bulić in Nejc Ilc



ASIC – popolnoma po meri: Intel 4004 (1971)

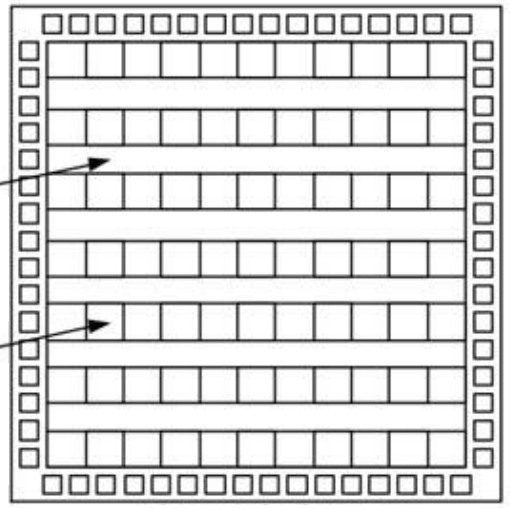
Full custom ASIC





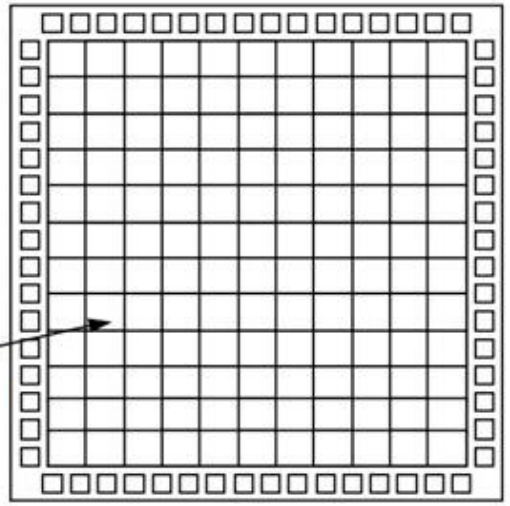
ASIC – delno po meri: CBIC (cell-based integrated circuit)

Semi-custom ASIC



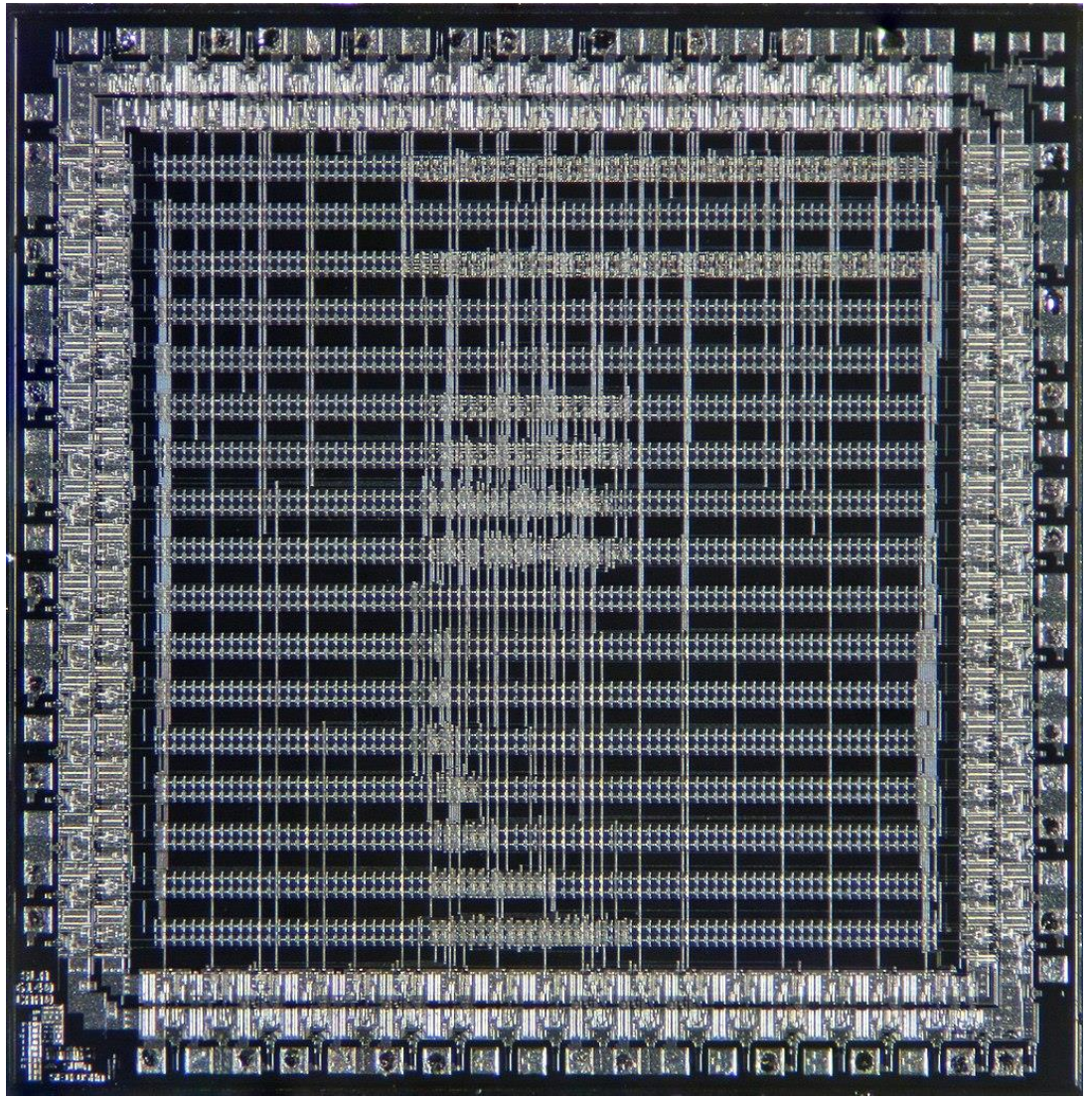
polje vrat s kanali

channeled gate array



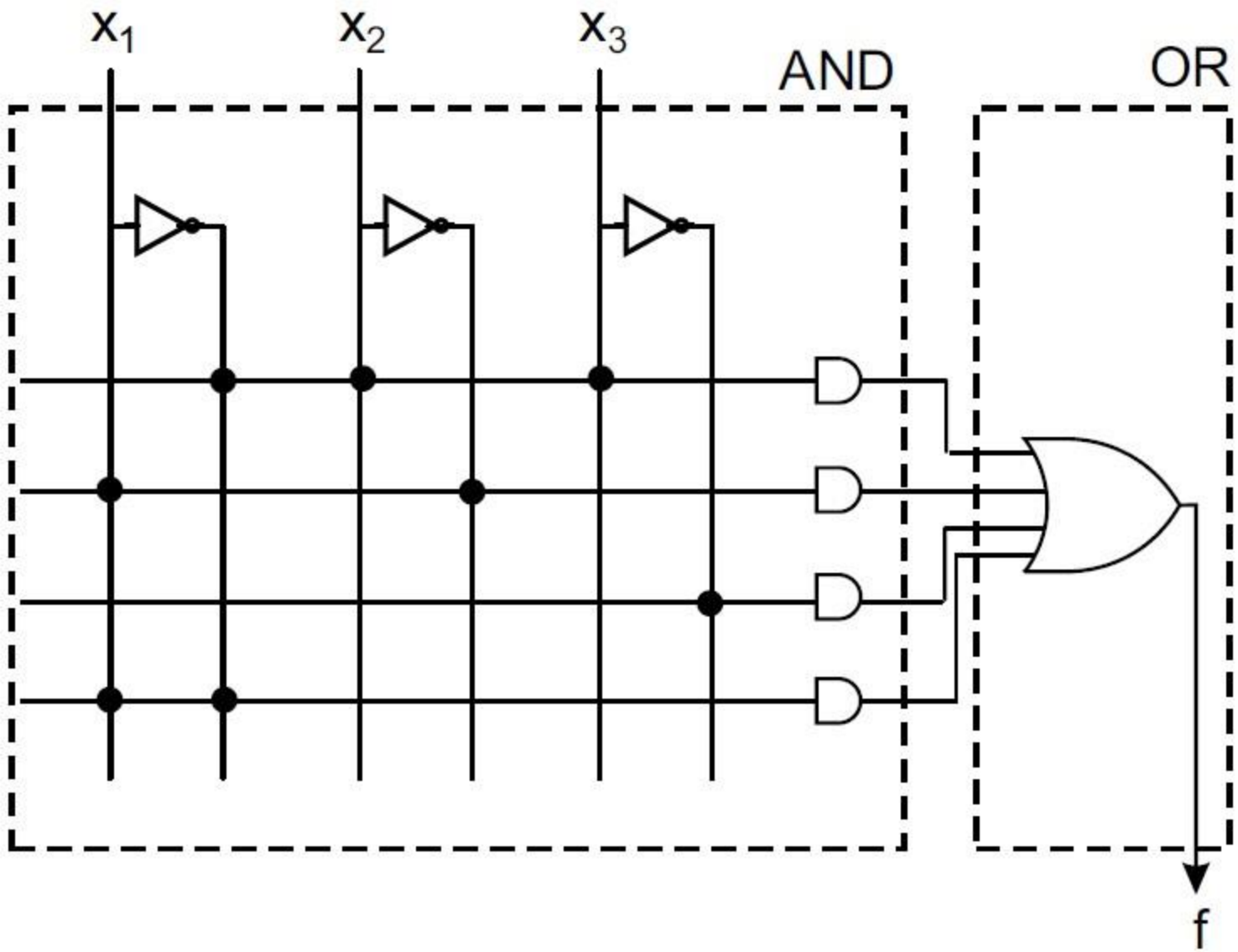
polje vrat brez kanalov

channel-less gate array

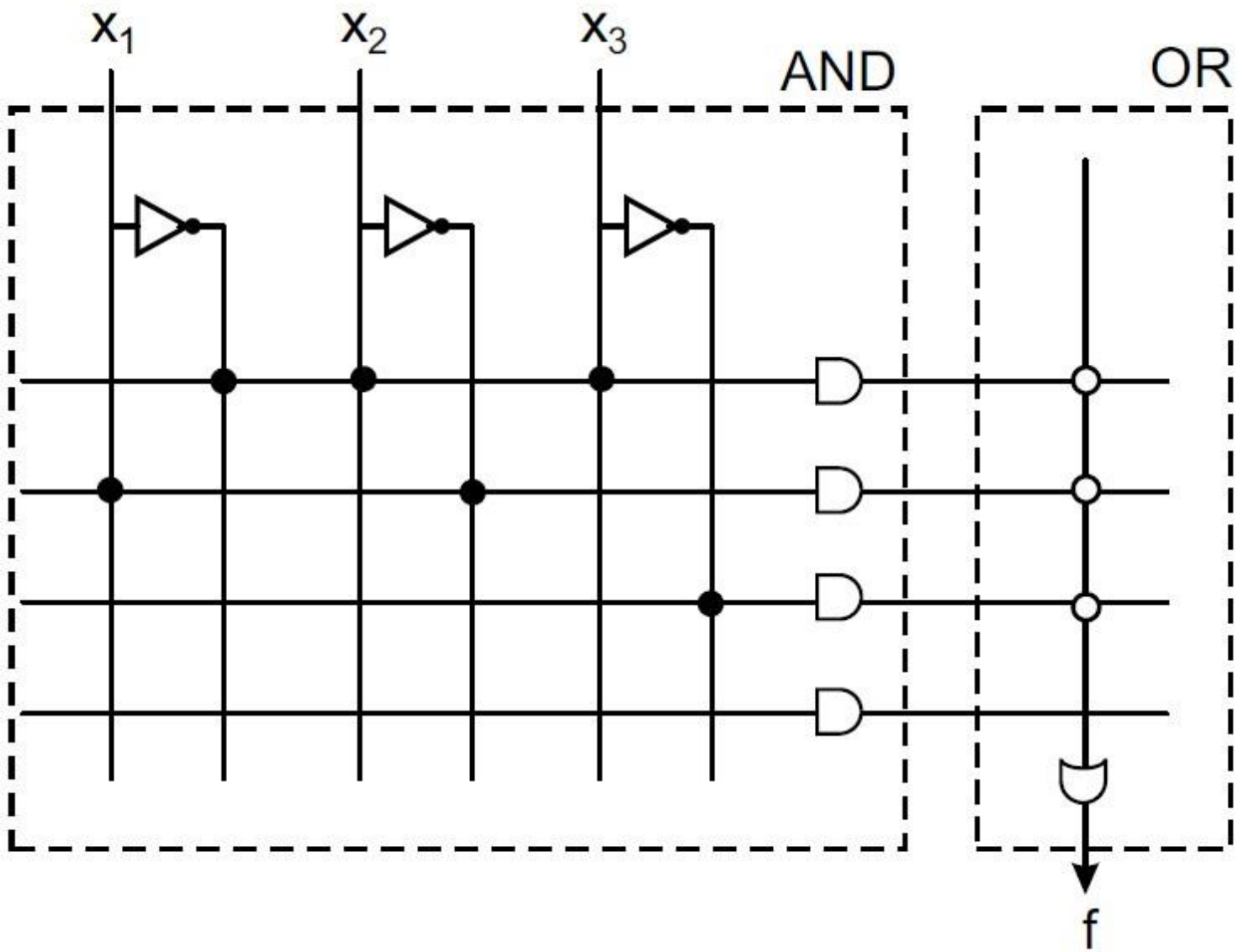


ASIC – delno po meri: polje vrat

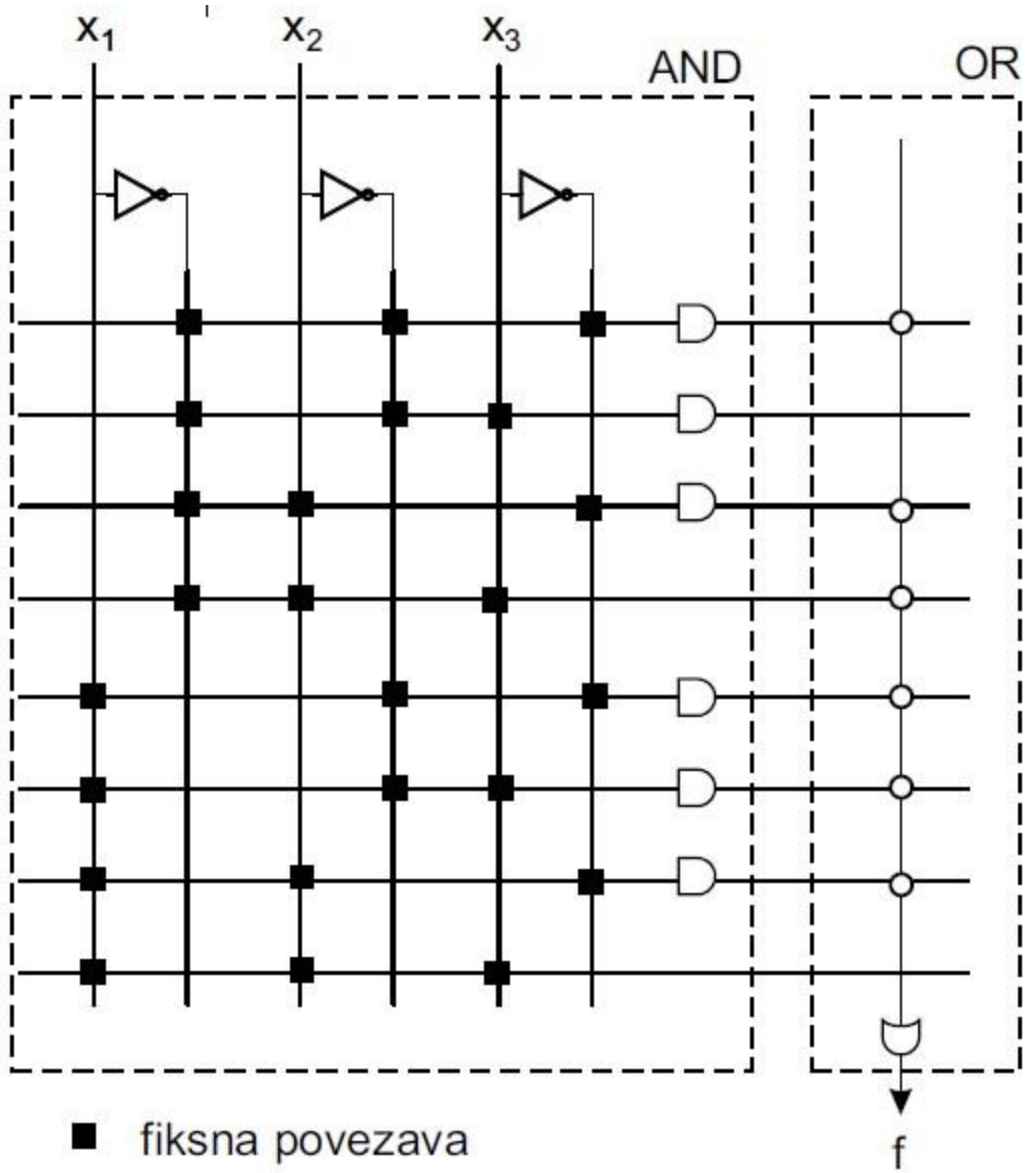
Semi-custom ASIC: gate array



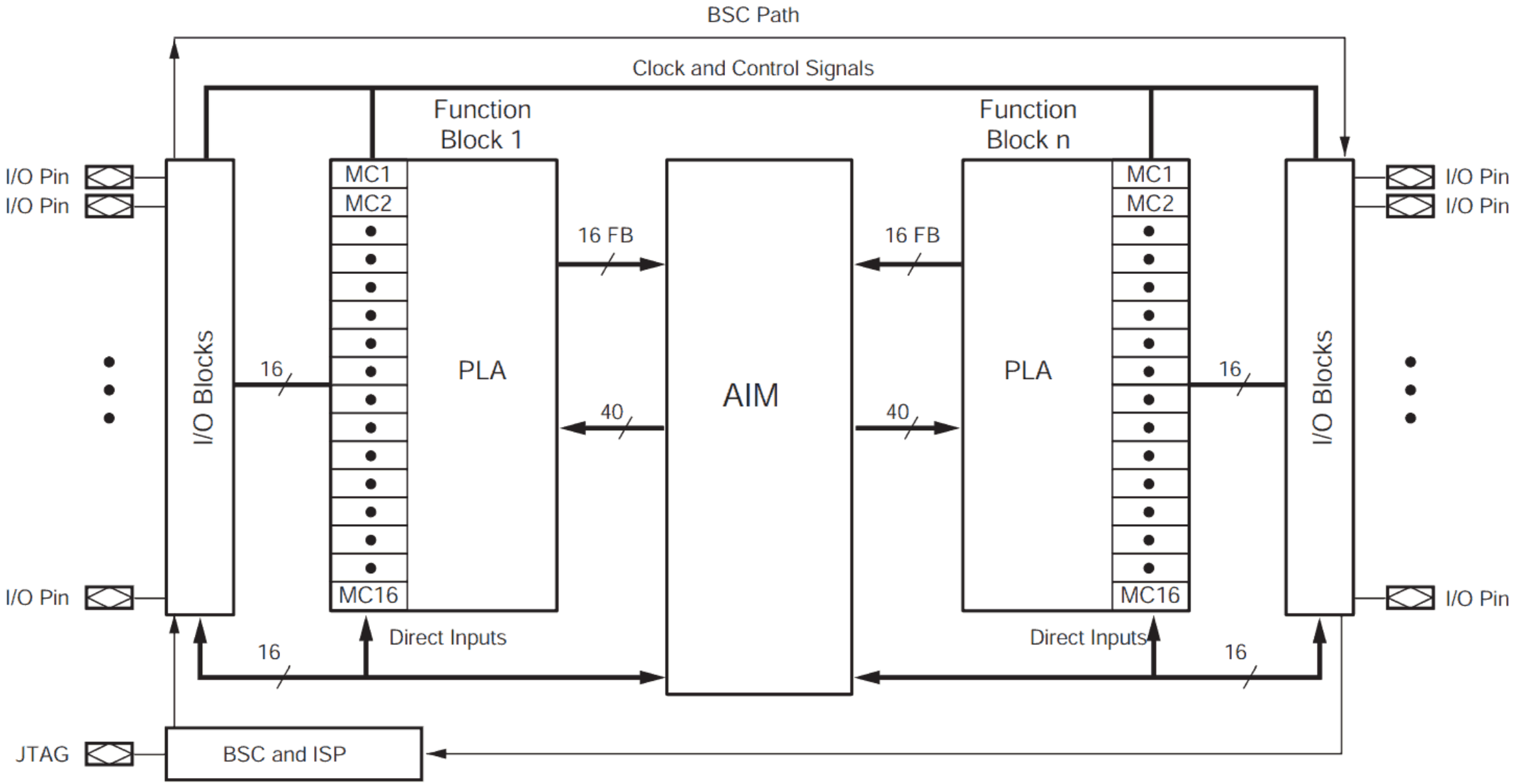
Programirljiv ASIC: PLD (programmable logic device) → PAL (programmable array logic)



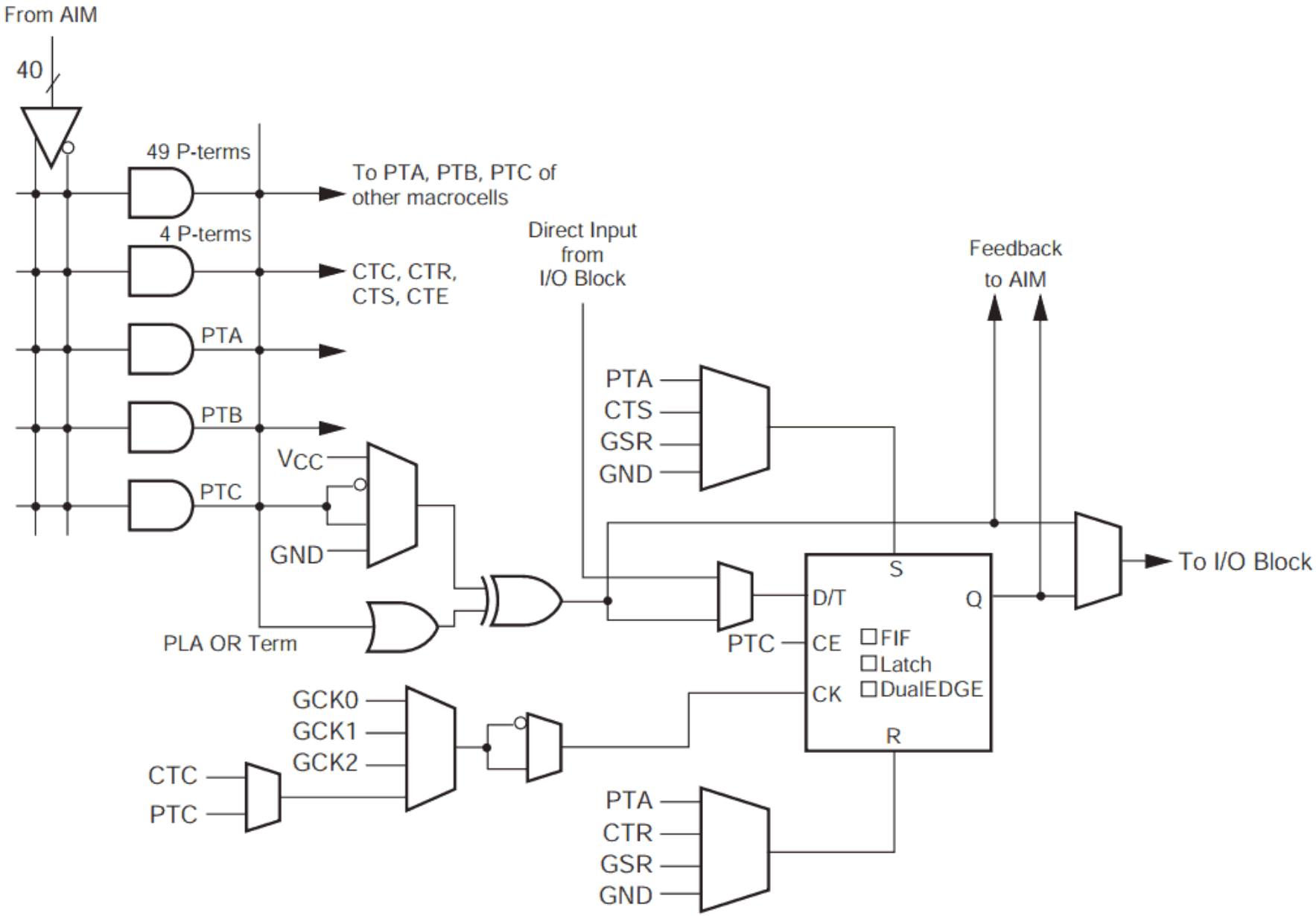
Programirljiv ASIC: PLD → PLA (programmable logic array)



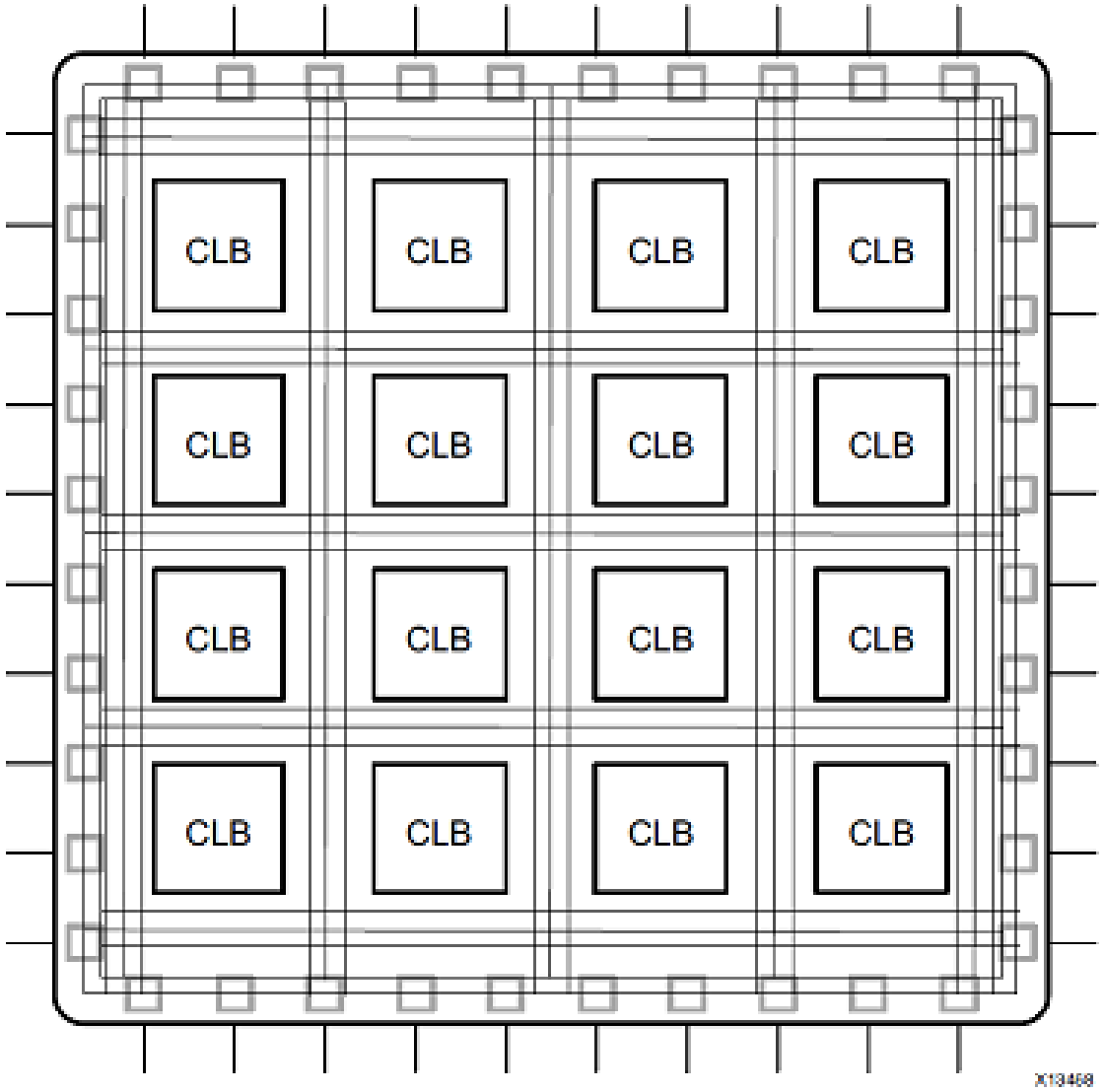
Programirljiv ASIC: PLD → PLE (programmable logic element)



Programirljiv ASIC: CPLD (complex PLD), primer Xilinx CoolRunner II

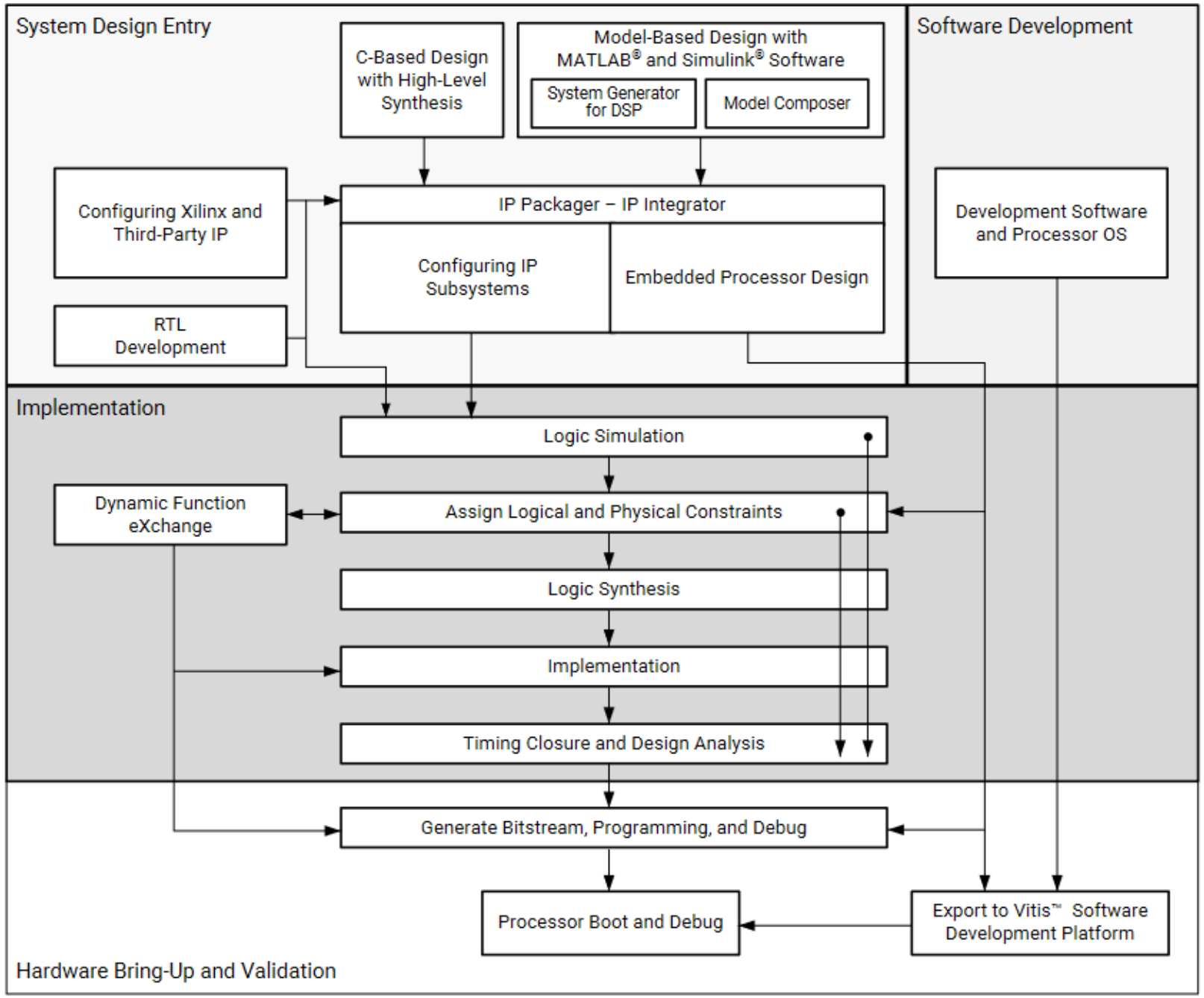


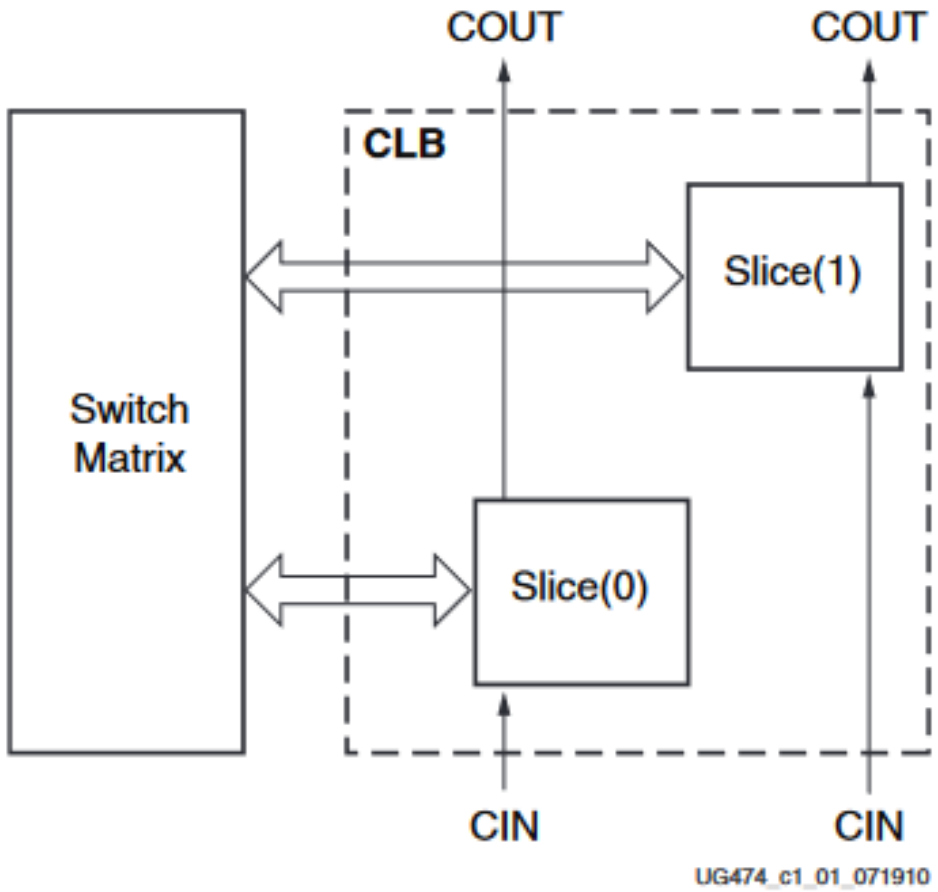
Xilinx CoolRunner II: makrocelica



Programirljiv ASIC: FPGA (field programmable gate array) - polje programirljivih vrat

Figure 1: **Vivado Design Suite High-Level Design Flow**




COUT
COUT
CLB
Switch
Matrix
Slice(1)
Slice(0)
CIN
CIN
UG474_c1_01_071910

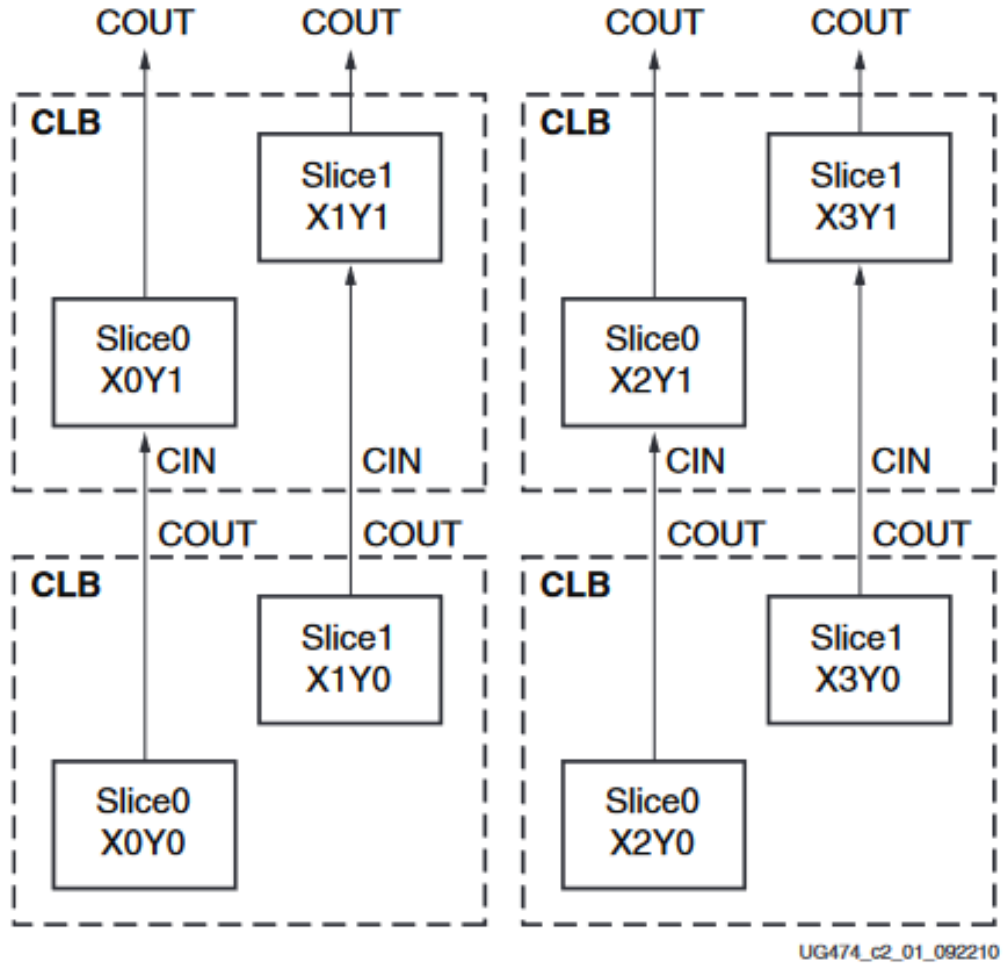

COUT
COUT
COUT
COUT
CLB
Slice1
X1Y1
Slice0
X0Y1
CIN
CIN
CLB
Slice1
X3Y1
Slice0
X2Y1
CIN
CIN
COUT
COUT
COUT
COUT
CLB
Slice1
X1Y0
Slice0
X0Y0
CLB
Slice1
X3Y0
Slice0
X2Y0
UG474_c2_01_092210

Table 1-2: **Artix-7 FPGA CLB Resources**

Device	Slices[1]	SLICEL	SLICEM	6-input LUTs	Distributed RAM (Kb)	Shift Register (Kb)	Flip-Flops
7A12T	2,000[2]	1,316	684	8,000	171	86	16,000
7A15T	2,600[2]	1,800	800	10,400	200	100	20,800
7A25T	3,650	2,400	1,250	14,600	313	156	29,200
7A35T	5,200[2]	3,600	1,600	20,800	400	200	41,600
7A50T	8,150	5,750	2,400	32,600	600	300	65,200
7A75T	11,800[2]	8,232	3,568	47,200	892	446	94,400
7A100T	15,850	11,100	4,750	63,400	1,188	594	126,800
7A200T	33,650	22,100	11,550	134,600	2,888	1,444	269,200

Notes:

1. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only SLICEMs can use their LUTs as distributed RAM or SRLs.
2. Number of slices corresponding to the number of LUTs and flip-flops supported in the device.

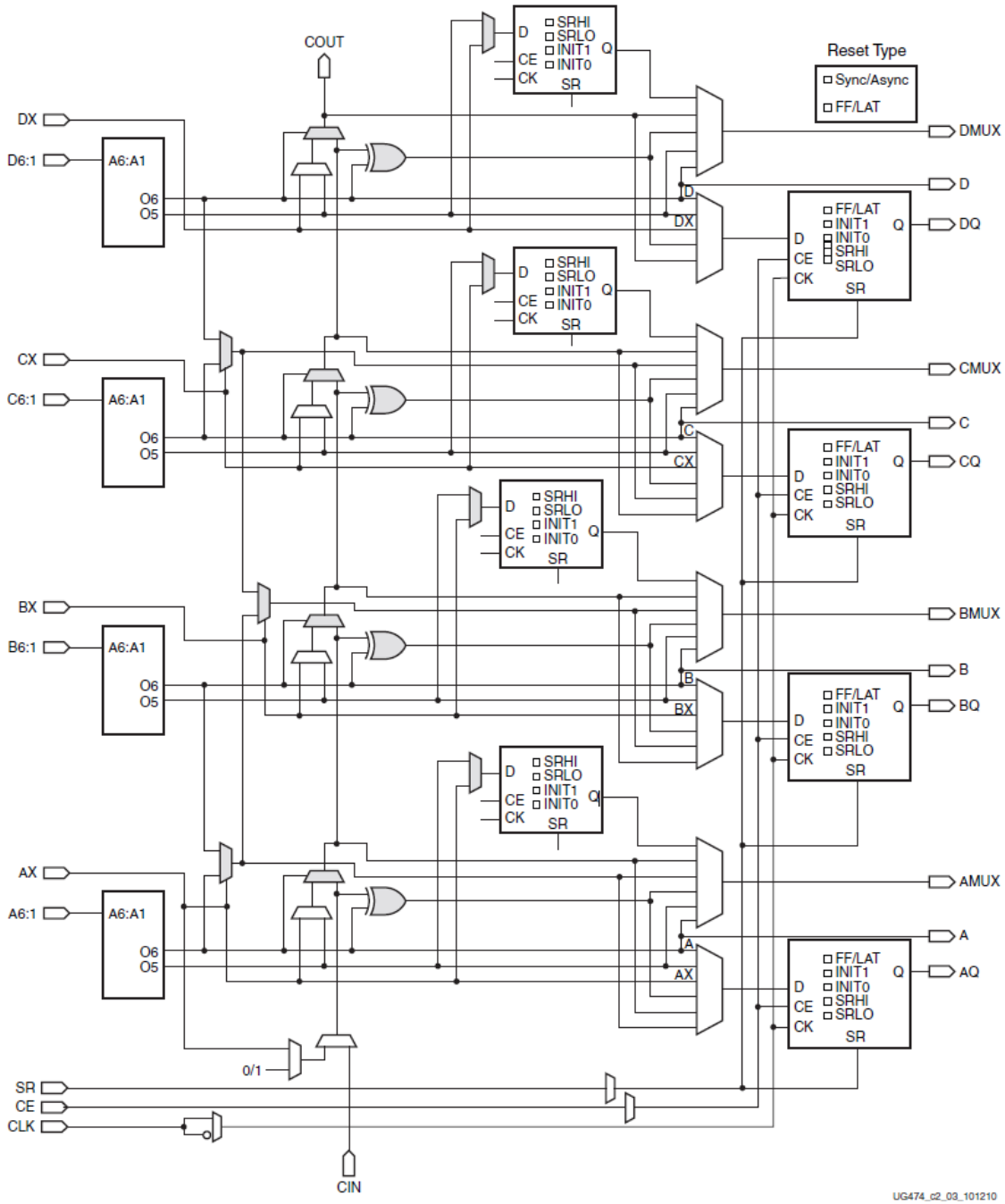


Figure 2-4: **Diagram of SLICEL**