

STM32H7

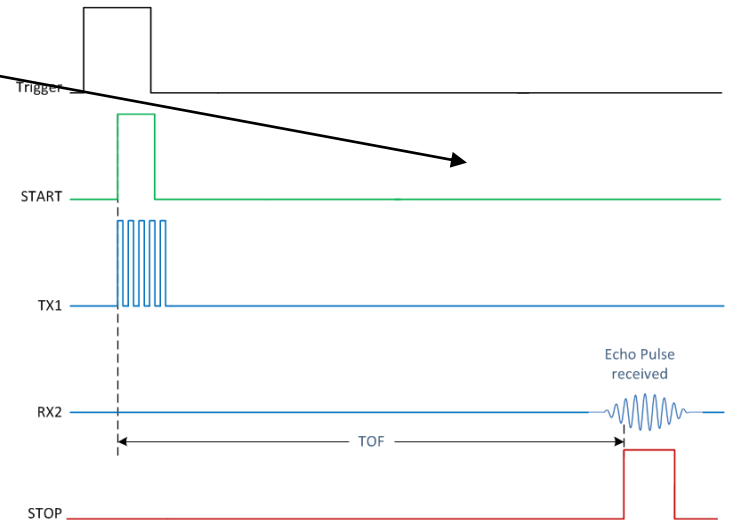
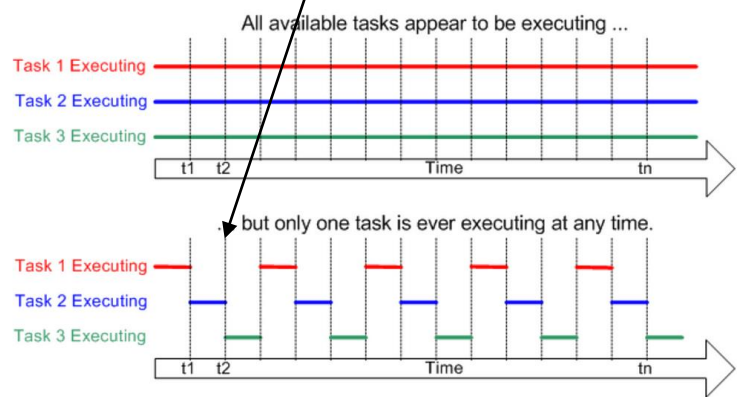
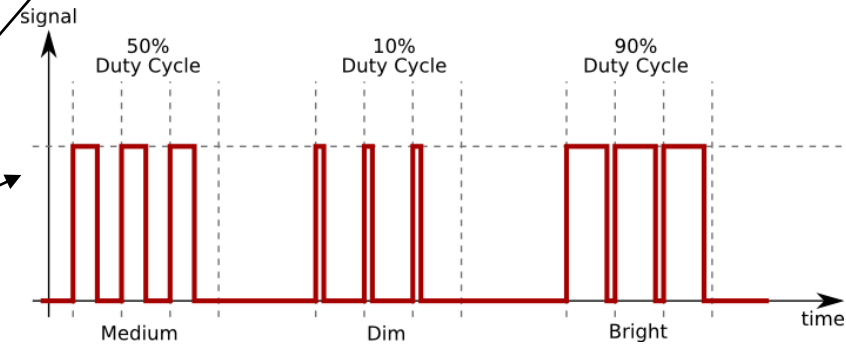
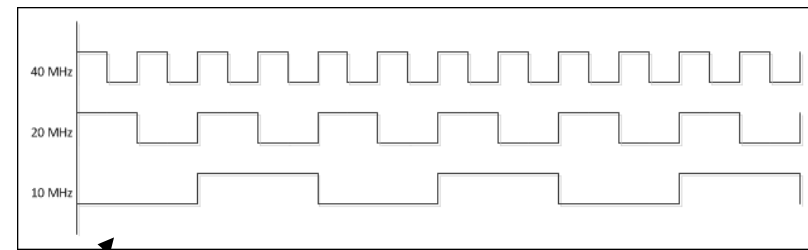
Vhodno / izhodne naprave

SysTick Časovnik

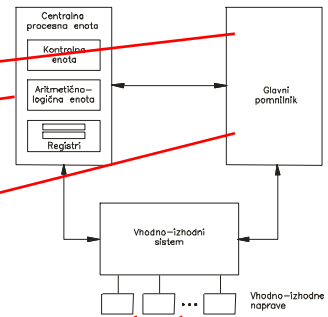
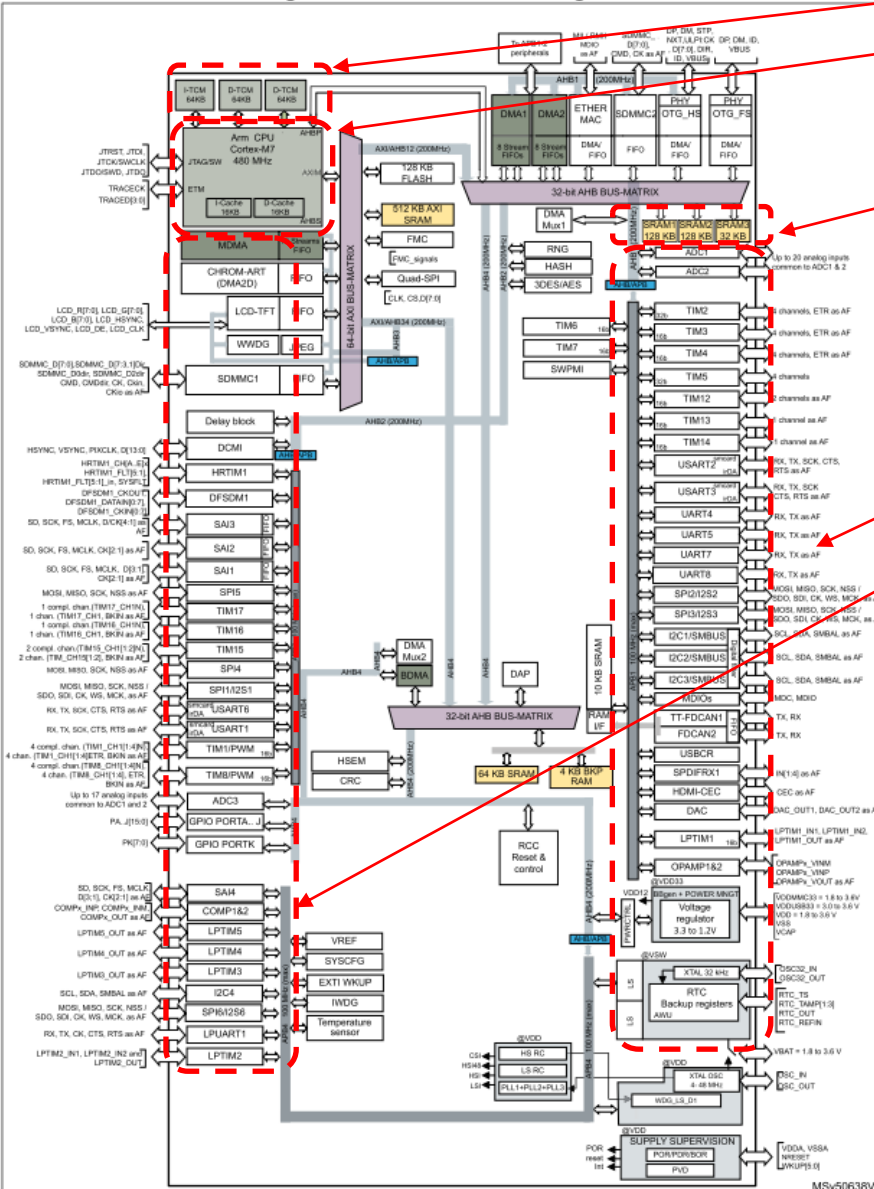
TC (časovnik / števec)

- Uporabni za štetje dogodkov
ali generiranje časovnih signalov (Waveform).

- zakasnitve (DELAY s časovnikom !)
- generiranje signala določene frekvence
- pulzno širinska modulacija (PWM)
- merjenje intervalov
- ciklične prekinitve!



STM32H750XB



Delo na STM32H7 razvojnem sistemu

Priključitev :

- **Mikro USB** priklp na **daljši stranici** (nad LCD, srednji !!!)

Poseben začetni projekt (github) in info za STM32H7 (e-učilnica):

- **dodajanje vsebine (Main.s):**



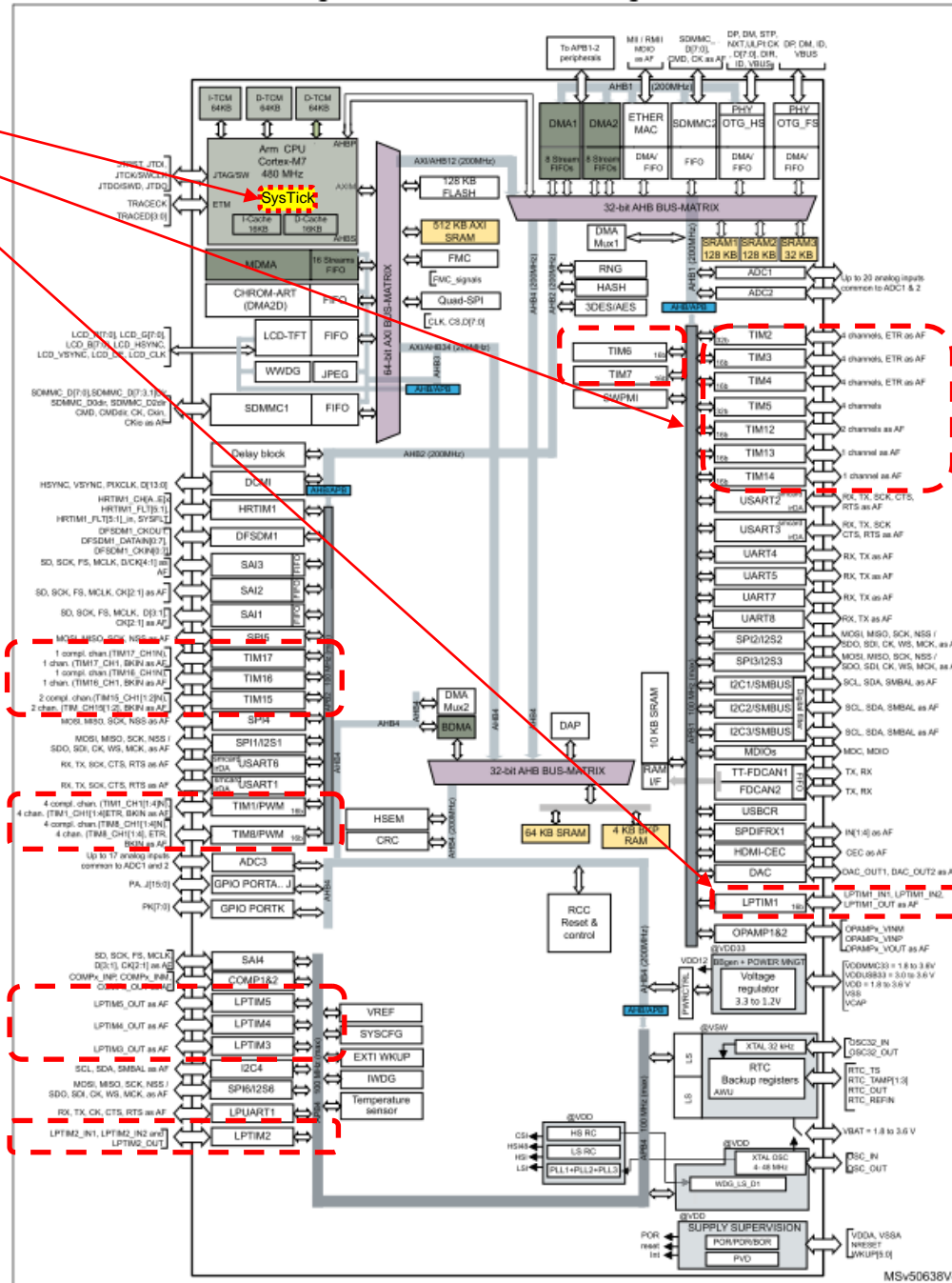
```
CubelDEWorkspace - stm32h7-asm/Core/Src/Main.s - STM32CubelDE
File Edit Source Refactor Navigate Search Project Run Window Help
Project Explorer x
CubelDE_Workspace
  stm32f4-asm-qemu
  Delo
    ARM9Template
    stm32f4-asm (in STM32AsmTemplate)
    ARM9Template.zip
    Node_V4 (in node_v4)
    Sluzba
      CAN_IEX_Module
      ORLab-STM32H7
        stm32h7-asm
          Binaries
          Includes
          Core
            Src
              Main.s
            Startup
              startup_stm32h750xbhx.s
          Debug
          out
          makefile
          README.md
          STM32H750X.svd
          STM32H750XBHX_FLASH.ld
          STM32H750XBHX_RAM.ld
          README.md
      RALab-STM32H7
        stm32h7-asm_RA_LED
          README.md
      STM32_USB_Key_AdvDebug
      STM32_USB_Key_FreeRTOS_AdvDebug
      STM32CubelDE_Adv_Debug
      STM32F4_Discovery_VIN_Projects

Main.s x startup_stm32h750xbhx.s
12
13 ////////////////////////////////////////////////////////////////////
14 // Definitions
15 ////////////////////////////////////////////////////////////////////
16 // Definitions section. Define all the registers and
17 // constants here for code readability.
18
19 // Constants
20
21
22 // Start of data section|
23     .data
24
25     .align
26
27 STEV1: .word  0x10 // 32-bitna spr.
28 STEV2: .word  0x40 // 32-bitna spr.
29 VSOTA: .word  0 // 32-bitna spr.
30
31
32 // Start of text section
33     .text
34
35     .type main, %function
36     .global main
37
38     .align
39 main:
40     ldr r0, =STEV1 // Naslov od STEV1 -> r0
41     ldr r1, [r0] // Vsebina iz naslova v r0 -> r1
42
43     ldr r0, =STEV2 // Naslov od STEV1 -> r0
44     ldr r2, [r0] // Vsebina iz naslova v r0 -> r2
45
46     add r3,r1,r2 // r1 + r2 -> r3
47
48     ldr r0, =VSOTA // Naslov od STEV1 -> r0
49     str r3,[r0] // iz registra r3 -> na naslov v r0
50
51 __end: b __end
52
```

----- Razvojni sistem STM32H750-DK -----

- STM32H750B-DK Discovery kit with STM32H750XB MCU
- ORLab-STM32H7 - GitHub repozitorij
- User Manual Discovery kit stm32h750xb Uploaded 11/11/22, 10.15
- DataSheet_stm32h750xb Uploaded 11/11/22, 10.16
- Reference Manual rm0433-stm32h750xb Uploaded 11/11/22, 10.17
- Programming_Manual_pm0253-stm32h750xb Uploaded 11/11/22, 10.17
- Errata_es0396-stm32h750xb Uploaded 11/11/22, 10.19

Časovniki



Vira: Reference & Programming manuals



PM0253 Programming manual

STM32F7 Series and STM32H7 Series Cortex[®]-M7 processor programming manual



RM0433 Reference manual

STM32H742, STM32H743/753 and STM32H750 Value line advanced Arm[®]-based 32-bit MCUs

PM0253 Cortex-M7 peripherals

4 Cortex-M7 peripherals

4.1 About the Cortex-M7 peripherals

The address map of the *Private peripheral bus* (PPB)

Core peripherals

PM0214

4.5 SysTick timer (STK)

0xE000E100-0xE000E4EF	Nested Vectored Interrupt Controller	Table 40 on page 184
0xE000ED00-0xE000ED3F	System control block	Table 50 on page 192
0xE000ED78-0xE000ED84	Processor features	Table 77 on page 217
0xE000ED90-0xE000EDB8	Memory Protection Unit	Table 84 on page 222
0xE000EF00-0xE000EF03	Nested Vectored Interrupt Controller	Table 40 on page 184
0xE000EF30-0xE000EF44	Floating-Point Unit	Table 94 on page 233
0xE000EF50-0xE000EF78	Cache maintenance operations	Table 100 on page 240
0xE000EF90-0xE000EFA8	Access control	Table 104 on page 245

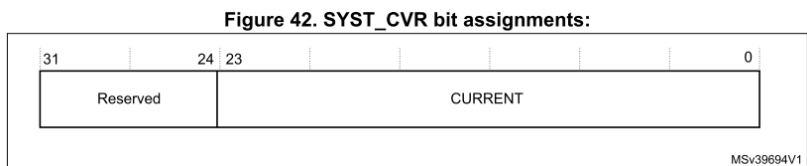
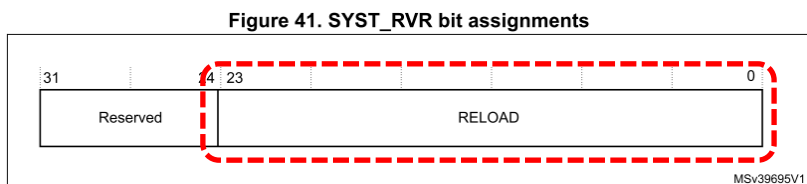
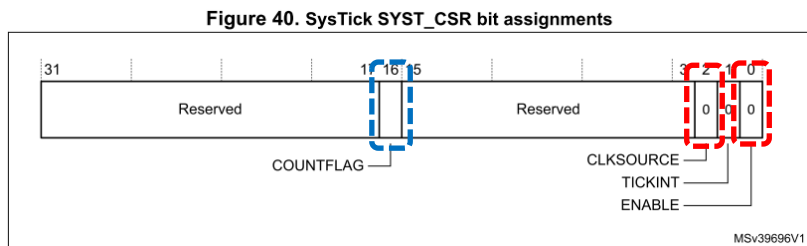
Table 71. System timer registers summary

Address	Name	Type	Required privilege	Reset value	Description
0xE000E010	SYST_CSR	RW	Privileged	0x00000004	<i>SysTick control and status register</i>
0xE000E014	SYST_RVR	RW	Privileged	UNKNOWN	<i>SysTick reload value register</i>
0xE000E018	SYST_CVR	RW	Privileged	UNKNOWN	<i>SysTick current value register</i>
0xE000E01C	SYST_CALIB	RO	Privileged	0xC0000000	<i>SysTick calibration value register</i>

37	High-Resolution Timer (HRTIM)	1371
38	Advanced-control timers (TIM1/TIM8)	1546
39	General-purpose timers (TIM2/TIM3/TIM4/TIM5)	1650
40	General-purpose timers (TIM12/TIM13/TIM14)	1726
41	General-purpose timers (TIM15/TIM16/TIM17)	1779
42	Basic timers (TIM6/TIM7)	1865
43	Low-power timer (LPTIM)	1878
44	System window watchdog (WWDG)	1907
45	Independent watchdog (IWDG)	1913
46	Real-time clock (RTC)	1923

SysTick časovnik – stanje, nastavitve

Bazni naslov za registre SysTick je 0xE000E010



Osnovni registri za delovanje SysTick časovnika:

SYST_CSR : vklop časovnika

CLKSOURCE=1, ENABLE=1

COUNTERFLAG=1, ko prešteje do 0 (postavi na SYST_RVR in nadaljuje)

SYST_RVR : zač. vrednost štetja (šteje proti 0)

SYST_RVR = število period

SYST_CVR : trenutna vrednost števca

SYST_CVR = nekje med SYST_RVR in 0

SysTick časovnik (Registri za nastavitve delovanja)

Figure 40. SysTick SYST_CSR bit assignments

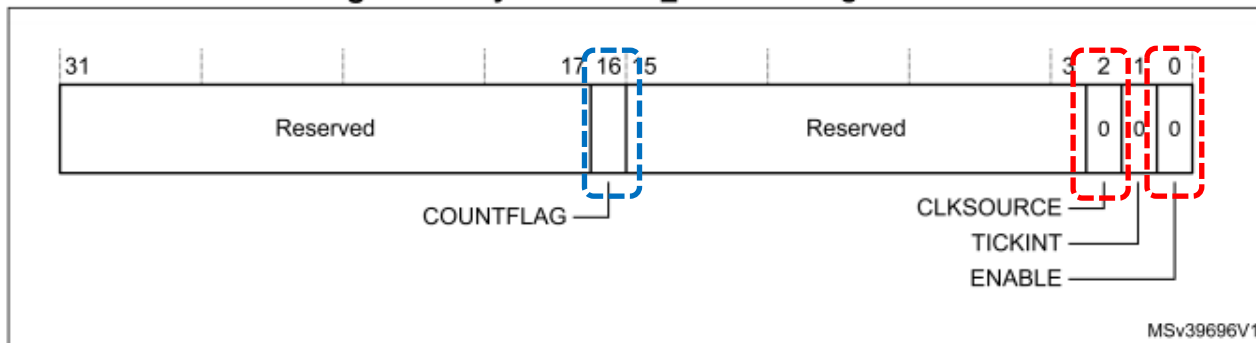


Table 72. SysTick SYST_CSR bit assignments

Bits	Name	Function
[31:17]	-	Reserved.
[16]	COUNTFLAG	Returns 1 if timer counted to 0 since last time this was read.
[15:3]	-	Reserved.
[2]	CLKSOURCE	Indicates the clock source: – 0: External clock. – 1: Processor clock.
[1]	TICKINT	Enables SysTick exception request: 0: Counting down to zero does not assert the SysTick exception request. 1: Counting down to zero asserts the SysTick exception request. Software can use COUNTFLAG to determine if SysTick has ever counted to zero.
[0]	ENABLE	Enables the counter: 0: Counter disabled. 1: Counter enabled.

SysTick časovnik (Registri za nastavitve delovanja)

4.4.2 SysTick reload value register

The SYST_RVR register specifies the start value to load into the SYST_CVR register. See the register summary in [Table 71 on page 213](#) for its attributes. The bit assignments are:

Figure 41. SYST_RVR bit assignments

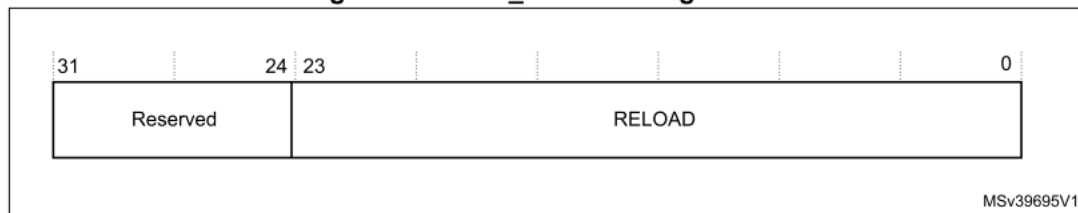


Table 73. SYST_RVR bit assignments

Bits	Name	Function
[31:24]	-	Reserved.
[23:0]	RELOAD	Value to load into the SYST_CVR register when the counter is enabled and when it reaches 0, see Calculating the RELOAD value .

Calculating the RELOAD value

The RELOAD value can be any value in the range 0x00000001-0x00FFFFFF. A start value of 0 is possible, but has no effect because the SysTick exception request and COUNTFLAG are activated when counting from 1 to 0.

The RELOAD value is calculated according to its use. For example, to generate a multi-shot timer with a period of N processor clock cycles, use a RELOAD value of N-1. If the SysTick interrupt is required every 100 clock pulses, set RELOAD to 99.

SysTick časovnik (Registri za nastavitve delovanja)

4.4.3 SysTick current value register

The SYST_CVR register contains the current value of the SysTick counter. See the register summary in [Table 71 on page 213](#) for its attributes. The bit assignments are

Figure 42. SYST_CVR bit assignments:

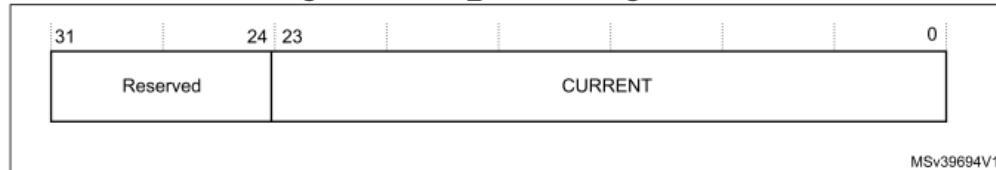


Table 74. SYST_CVR bit assignments

Bits	Name	Function
[31:24]	-	Reserved.
[23:0]	CURRENT	Reads return the current value of the SysTick counter. A write of any value clears the field to 0, and also clears the SYST_CSR COUNTFLAG bit to 0.

SysTick Časovnik – krmiljenje

Potrebni koraki za krmiljenje časovnika SysTick:

1. **SYST_RVR** (Reload Value Register): **Value** SYSTICK_RELOAD_1MS
2. **SYST_CVR** (Current Value Register): **0, reset to zero**
3. **SYST_CSR** (Control/Status Register): **0b101 : Proc. Clock, enable**
-> **Start SysTick**



4. Delovanje:

Čakanje na pojavitev COUNT_FLAG=1 (b₁₆) v SYST_CSR



Naslovi registrov:

```
// SysTick Timer definitions
.equ     SCS_BASE, 0xe000e000
.equ     SCS_SYST_CSR, 0x10 // Control/Status register
.equ     SCS_SYST_RVR, 0x14 // Value to countdown from
.equ     SCS_SYST_CVR, 0x18 // Current value

.equ     SYSTICK_RELOAD_1MS,      63999 //1 msec at 64MHz ...
```

SysTick časovnik

H7 : SysTick

LODŠTEVA : RVR → \emptyset



















		(64000-1)	BAŽNI NASLOV	OPIS
①	SYST_RVR	63999	SCS_BASE	RELOAD VALUE (ZG. MEJA)
②	SYST_CVR	0	"	ZAČ. VREDNOST
③	SYST_CSR	CLK SOURCE 1 b2	ENABLE 1 b0	ZAGON
DELO TANJE 4	SYST_CSR	COUNT FLAG 1 b16		PRETEK ŠTETJA

VRIN SIGNAL

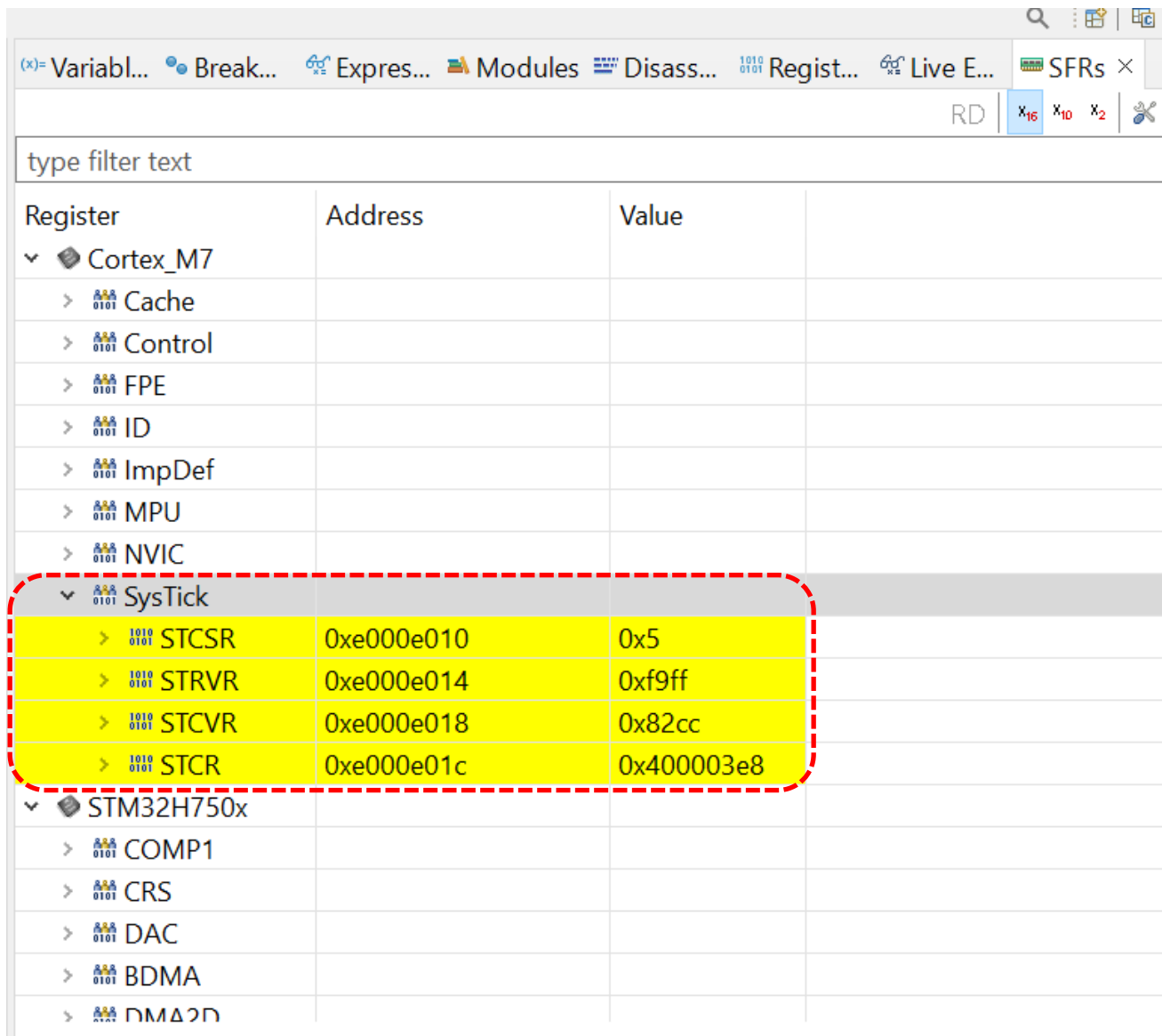
$f_{CPU} = 64MHz$ per/s 64000000 per/ms 64000

DEF

CubeIDE – Registers okno

Name	Value
▼  0101 General Registers	
 0101 r0	0x0
 0101 r1	0x0
 0101 r2	0x0
 0101 r3	0x0
 0101 r4	0x0
 0101 r5	0x1000
 0101 r6	0x40020c14
 0101 r7	0x0
 0101 r8	0x0
 0101 r9	0x0
 0101 r10	0x0
 0101 r11	0x0
 0101 r12	0x0
 0101 sp	0x20020000
 0101 lr	0xffffffff
 0101 pc	0x800002a
 0101 xpsr	0x41000000

CubeIDE – SFR okno



type filter text

Register	Address	Value
▼ Cortex_M7		
> Cache		
> Control		
> FPE		
> ID		
> ImpDef		
> MPU		
> NVIC		
▼ SysTick		
> STCSR	0xe000e010	0x5
> STRVR	0xe000e014	0xf9ff
> STCVR	0xe000e018	0x82cc
> STCR	0xe000e01c	0x400003e8
▼ STM32H750x		
> COMP1		
> CRS		
> DAC		
> BDMA		
> DMA2D		

Utripanje LED diode – s časovnikom :

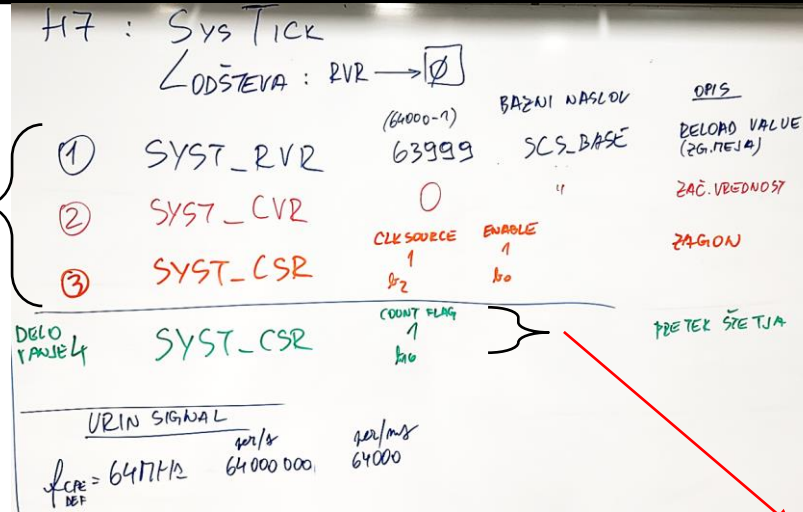
main:

```
b1 INIT_IO // Priprava za kontrolo LED diode  
b1 INIT_TC // Priprava SysTick časovnika
```

loop:

```
b1 LED_ON // Vklop LED diode  
  
mov r0,#500  
// b1 DELAY // Zakasnitev SW Delay: r0 x 1msec  
b1 DELAYTC // Zakasnitev SysTick : r0 x 1msec  
  
b1 LED_OFF // Izlop LED diode  
  
mov r0,#500  
// b1 DELAY // Zakasnitev SW Delay: r0 x 1msec  
b1 DELAYTC // Zakasnitev SysTick : r0 x 1msec  
  
b loop // skok na vrstico loop:
```

Utripanje LED diode – s časovnikom :



INIT_TC:

```

push {r0, r1, lr}
ldr r1, =SCS_BASE

ldr r0, =SYSTICK_RELOAD_1MS
str r0, [r1, #SCS_SYST_RVR]

mov r0, #0
str r0, [r1, #SCS_SYST_CVR]

mov r0, #0b101
str r0, [r1, #SCS_SYST_CSR]

pop {r0, r1, pc}
    
```

// Delay with internal timer based loop approx.

r0 x ms

DELAYTC:

```

push {r1, r2, lr}
ldr r1, =SCS_BASE
    
```

```

LOOPTC:  ldr r2, [r1, #SCS_SYST_CSR]
         tst r2, #0x10000 // COUNT_FLAG=1?
         beq LOOPTC
    
```

```

         subs r0, r0, #1
         bne LOOPTC
pop {r1, r2, pc}
    
```