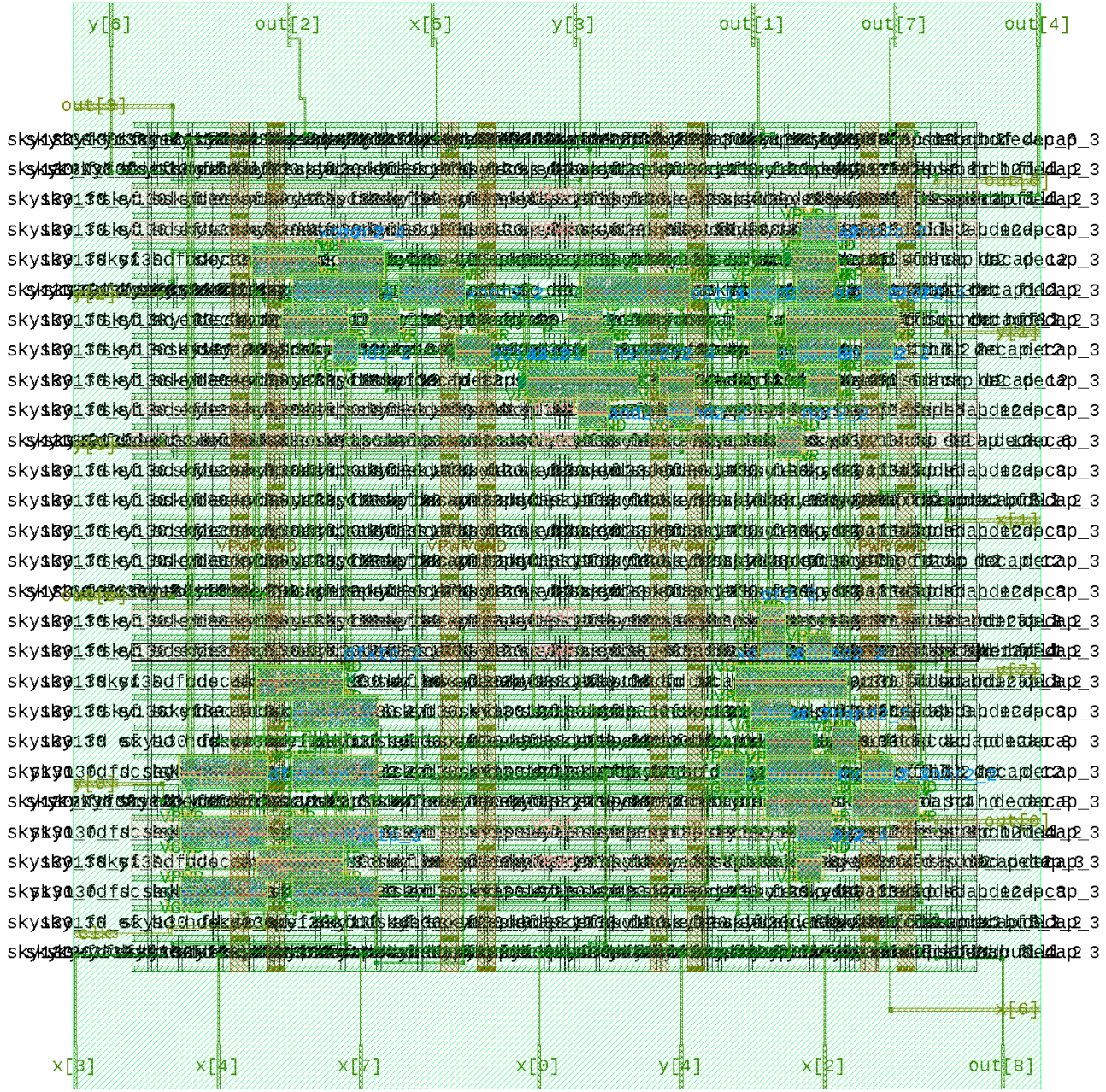
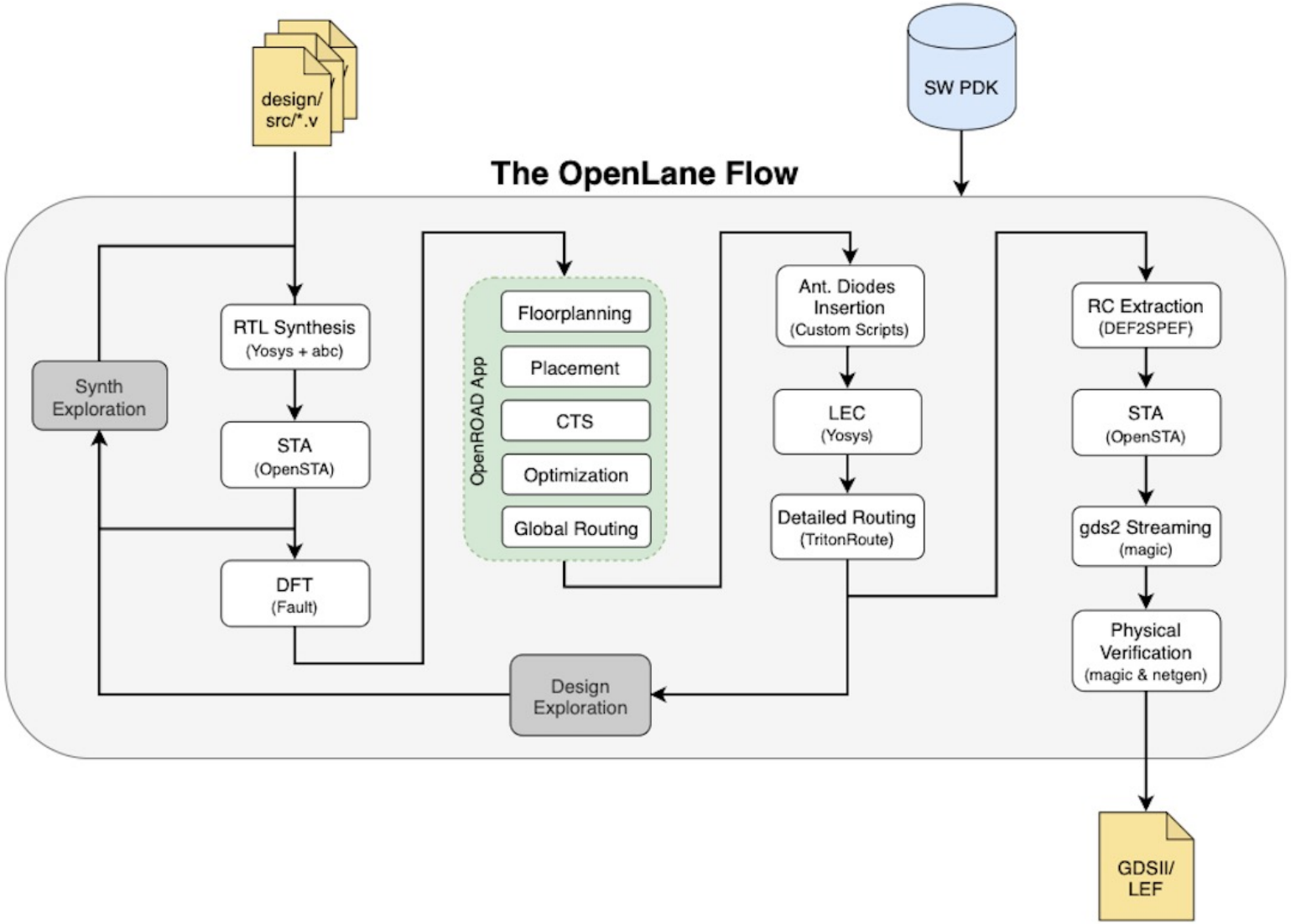
Načrtovanje ASIC digitalnih vezij z orodjem OpenLANE

RTL2GDS

```
module registeredNAND4(a_in, b_in, ce, clk, rst, dout);
  input [3:0] a_in;
  input [3:0] b_in;
  input ce;
  input clk;
  input rst;
  output [3:0] dout;

  reg [3:0] d_reg;

  always @ (posedge clk)
    begin
      if(rst)
        d_reg <= 4'b0;
    else if(ce)
      d_reg <= ~(a_in & b_in);
    end
    assign dout = d_reg;
endmodule
```

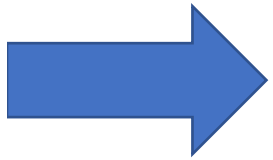


OpenLane tok



Sinteza (Verilog -> Verilog Std Cells)

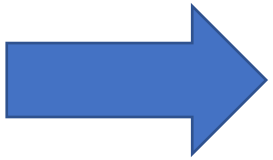
```
module registeredNAND4(a_in, b_in, ce, clk, rst, dout);
  input [3:0] a_in;
  input [3:0] b_in;
  input ce;
  input clk;
  input rst;
  output [3:0] dout;

  reg [3:0] d_reg;

  always @ (posedge clk)
    begin
      if(rst)
        d_reg <= 4'b0;
    else if(ce)
      d_reg <= ~(a_in & b_in);
    end
    assign dout = d_reg;
endmodule
```



```
input ce;
wire ce;
input clk;
wire clk;
output [3:0] dout;
wire [3:0] dout;
input rst;
wire rst;
sky130_fd_sc_hd__inv_2 _18_ (
  .A(a_in[3]),
  .Y(_04_)
);
sky130_fd_sc_hd__nand2_2 _19_ (
  .A(ce),
  .B(b_in[3]),
  .Y(_05_)
);
sky130_fd_sc_hd__nor2_2 _20_ (
  .A(_04_),
  .B(_05_),
  .Y(_06_)
);
sky130_fd_sc_hd__o21bai_2 _21_ (
  .A1(ce),
  .A2(dout[3]),
  .B1_N(rst),
  .Y(_07_)
);
sky130_fd_sc_hd__nor2_4 _22_ (
  .A(_06_),
  .B(_07_),
  .Y(_00_)
);
sky130_fd_sc_hd__inv_2 _23_ (
  .A(ce),
  .Y(_08_)
);
sky130_fd_sc_hd__nand2_2 _24_ (
  .A(b_in[0]),
  .B(a_in[0]),
  .Y(_09_)
);
```

(FLOORPLAN: Verilog Std Cells + Vias + Pins… -> Floor)

```
input ce;
wire ce;
input clk;
wire clk;
output [3:0] dout;
wire [3:0] dout;
input rst;
wire rst;
sky130_fd_sc_hd__inv_2 _18_ (
  .A(a_in[3]),
  .Y(_04_)
);
sky130_fd_sc_hd__nand2_2 _19_ (
  .A(ce),
  .B(b_in[3]),
  .Y(_05_)
);
sky130_fd_sc_hd__nor2_2 _20_ (
  .A(_04_),
  .B(_05_),
  .Y(_06_)
);
sky130_fd_sc_hd__o21bai_2 _21_ (
  .A1(ce),
  .A2(dout[3]),
  .B1_N(rst),
  .Y(_07_)
);
sky130_fd_sc_hd__nor2_4 _22_ (
  .A(_06_),
  .B(_07_),
  .Y(_00_)
);
sky130_fd_sc_hd__inv_2 _23_ (
  .A(ce),
  .Y(_08_)
);
sky130_fd_sc_hd__nand2_2 _24_ (
  .A(b_in[0]),
  .B(a_in[0]),
  .Y(_09_)
);
```



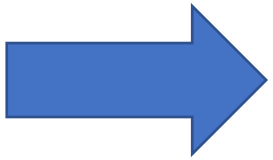
DEF: (placement and conectivity)
- die area
- macros
- components
- metal layers
- vias
- pins…

```
DESIGN registeredNAND4 ;
UNITS DISTANCE MICRONS 1000 ;
DIEAREA ( 0 0 ) ( 226780 237500 ) ;
ROW ROW_0 unithd 5520 10880 N DO 469 BY 1 STEP 460 0 ;
ROW ROW_1 unithd 5520 13600 FS DO 469 BY 1 STEP 460 0 ;
ROW ROW_2 unithd 5520 16320 N DO 469 BY 1 STEP 460 0 ;
```

```
    - _18_ sky130_fd_sc_hd__inv_2 ;
    - _19_ sky130_fd_sc_hd__nand2_2 ;
    - _20_ sky130_fd_sc_hd__nor2_2 ;
    - _21_ sky130_fd_sc_hd__o21bai_2 ;
    - _22_ sky130_fd_sc_hd__nor2_4 ;
    - _23_ sky130_fd_sc_hd__inv_2 ;
    - _24_ sky130_fd_sc_hd__nand2_2 ;
    - _25_ sky130_fd_sc_hd__nor2_2 ;
    - _26_ sky130_fd_sc_hd__o21bai_2 ;
    - _27_ sky130_fd_sc_hd__nor2_4 ;
    - _28_ sky130_fd_sc_hd__nand2_2 ;
    - _29_ sky130_fd_sc_hd__nor2_2 ;
    - _30_ sky130_fd_sc_hd__o21bai_2 ;
    - _31_ sky130_fd_sc_hd__nor2_4 ;
    - _32_ sky130_fd_sc_hd__nand2_2 ;
    - _33_ sky130_fd_sc_hd__nor2_2 ;
    - _34_ sky130_fd_sc_hd__o21bai_2 ;
    - _35_ sky130_fd_sc_hd__nor2_4 ;
    - _36_ sky130_fd_sc_hd__dfxtp_2 ;
    - _37_ sky130_fd_sc_hd__dfxtp_2 ;
    - _38_ sky130_fd_sc_hd__dfxtp_2 ;
    - _39_ sky130_fd_sc_hd__dfxtp_2 ;
END COMPONENTS
```

(PLACEMENT: Verilog Std Cells + Vias + Pins… -> Place)

```
input ce;
wire ce;
input clk;
wire clk;
output [3:0] dout;
wire [3:0] dout;
input rst;
wire rst;
sky130_fd_sc_hd__inv_2 _18_ (
  .A(a_in[3]),
  .Y(_04_)
);
sky130_fd_sc_hd__nand2_2 _19_ (
  .A(ce),
  .B(b_in[3]),
  .Y(_05_)
);
sky130_fd_sc_hd__nor2_2 _20_ (
  .A(_04_),
  .B(_05_),
  .Y(_06_)
);
sky130_fd_sc_hd__o21bai_2 _21_ (
  .A1(ce),
  .A2(dout[3]),
  .B1_N(rst),
  .Y(_07_)
);
sky130_fd_sc_hd__nor2_4 _22_ (
  .A(_06_),
  .B(_07_),
  .Y(_00_)
);
sky130_fd_sc_hd__inv_2 _23_ (
  .A(ce),
  .Y(_08_)
);
sky130_fd_sc_hd__nand2_2 _24_ (
  .A(b_in[0]),
  .B(a_in[0]),
  .Y(_09_)
);
```



```
DESIGN registeredNAND4 ;
UNITS DISTANCE MICRONS 1000 ;
DIEAREA ( 0 0 ) ( 226780 237500 ) ;
ROW ROW_0 unithd 5520 10880 N DO 469 BY 1 STEP 460 0 ;
ROW ROW_1 unithd 5520 13600 FS DO 469 BY 1 STEP 460 0 ;
ROW ROW_2 unithd 5520 16320 N DO 469 BY 1 STEP 460 0 ;
```

```
- input1 sky130_fd_sc_hd__buf_1 + SOURCE TIMING + PLACED ( 218500 138720 ) S ;
- input10 sky130_fd_sc_hd__clkbuf_2 + SOURCE TIMING + PLACED ( 218040 78880 ) S ;
- input2 sky130_fd_sc_hd__buf_1 + SOURCE TIMING + PLACED ( 74520 223040 ) N ;
- input3 sky130_fd_sc_hd__buf_1 + SOURCE TIMING + PLACED ( 180780 10880 ) FN ;
- input4 sky130_fd_sc_hd__buf_1 + SOURCE TIMING + PLACED ( 135700 223040 ) FN ;
- input5 sky130_fd_sc_hd__clkbuf_2 + SOURCE TIMING + PLACED ( 6900 10880 ) N ;
- input6 sky130_fd_sc_hd__buf_1 + SOURCE TIMING + PLACED ( 6900 125120 ) N ;
- input7 sky130_fd_sc_hd__buf_1 + SOURCE TIMING + PLACED ( 58420 10880 ) N ;
- input8 sky130_fd_sc_hd__dlymetal6s2s_1 + SOURCE TIMING + PLACED ( 215280 13600 ) S ;
- input9 sky130_fd_sc_hd__clkbuf_4 + SOURCE TIMING + PLACED ( 6900 62560 ) FS ;
- output11 sky130_fd_sc_hd__clkbuf_4 + SOURCE TIMING + PLACED ( 199180 223040 ) N ;
- output12 sky130_fd_sc_hd__clkbuf_4 + SOURCE TIMING + PLACED ( 121900 10880 ) N ;
- output13 sky130_fd_sc_hd__buf_2 + SOURCE TIMING + PLACED ( 6900 190400 ) FN ;
- output14 sky130_fd_sc_hd__clkbuf_4 + SOURCE TIMING + PLACED ( 18860 223040 ) FN ;
COMPONENTS
```

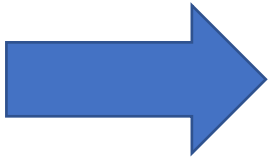
DEF: (placement and conectivity)

- die area
- macros
- components
- metal layers
- vias
- pins…

```
PINS 17 ;
    - VGND + NET VGND + SPECIAL + DIRECTION INOUT + USE GROUND
      + PORT
        + LAYER met5 ( -108110 -800 ) ( 108110 800 )
        + LAYER met5 ( -108110 -153980 ) ( 108110 -152380 )
        + LAYER met4 ( 64550 -173370 ) ( 66150 41990 )
        + LAYER met4 ( -89050 -173370 ) ( -87450 41990 )
        + FIXED ( 113390 184010 ) N ;
    - VPWR + NET VPWR + SPECIAL + DIRECTION INOUT + USE POWER
      + PORT
        + LAYER met5 ( -108110 -800 ) ( 108110 800 )
        + LAYER met5 ( -108110 -153980 ) ( 108110 -152380 )
        + LAYER met4 ( 61250 -170070 ) ( 62850 45290 )
        + LAYER met4 ( -92350 -170070 ) ( -90750 45290 )
        + FIXED ( 113390 180710 ) N ;
```

RC Extraction: Physical (shape) –> Electrical (R,C) (DEF -> Spice)

```
- input1 sky130_fd_sc_hd__buf_1 + SOURCE TIMING + PLACED ( 218500 138720 ) S ;
- input10 sky130_fd_sc_hd__clkbuf_2 + SOURCE TIMING + PLACED ( 218040 78880 ) S ;
- input2 sky130_fd_sc_hd__buf_1 + SOURCE TIMING + PLACED ( 74520 223040 ) N ;
- input3 sky130_fd_sc_hd__buf_1 + SOURCE TIMING + PLACED ( 180780 10880 ) FN ;
- input4 sky130_fd_sc_hd__buf_1 + SOURCE TIMING + PLACED ( 135700 223040 ) FN ;
- input5 sky130_fd_sc_hd__clkbuf_2 + SOURCE TIMING + PLACED ( 6900 10880 ) N ;
- input6 sky130_fd_sc_hd__buf_1 + SOURCE TIMING + PLACED ( 6900 125120 ) N ;
- input7 sky130_fd_sc_hd__buf_1 + SOURCE TIMING + PLACED ( 58420 10880 ) N ;
- input8 sky130_fd_sc_hd__dlymetal6s2s_1 + SOURCE TIMING + PLACED ( 215280 13600 ) S ;
- input9 sky130_fd_sc_hd__clkbuf_4 + SOURCE TIMING + PLACED ( 6900 62560 ) FS ;
- output11 sky130_fd_sc_hd__clkbuf_4 + SOURCE TIMING + PLACED ( 199180 223040 ) N ;
- output12 sky130_fd_sc_hd__clkbuf_4 + SOURCE TIMING + PLACED ( 121900 10880 ) N ;
- output13 sky130_fd_sc_hd__buf_2 + SOURCE TIMING + PLACED ( 6900 190400 ) FN ;
- output14 sky130_fd_sc_hd__clkbuf_4 + SOURCE TIMING + PLACED ( 18860 223040 ) FN ;
COMPONENTS
```



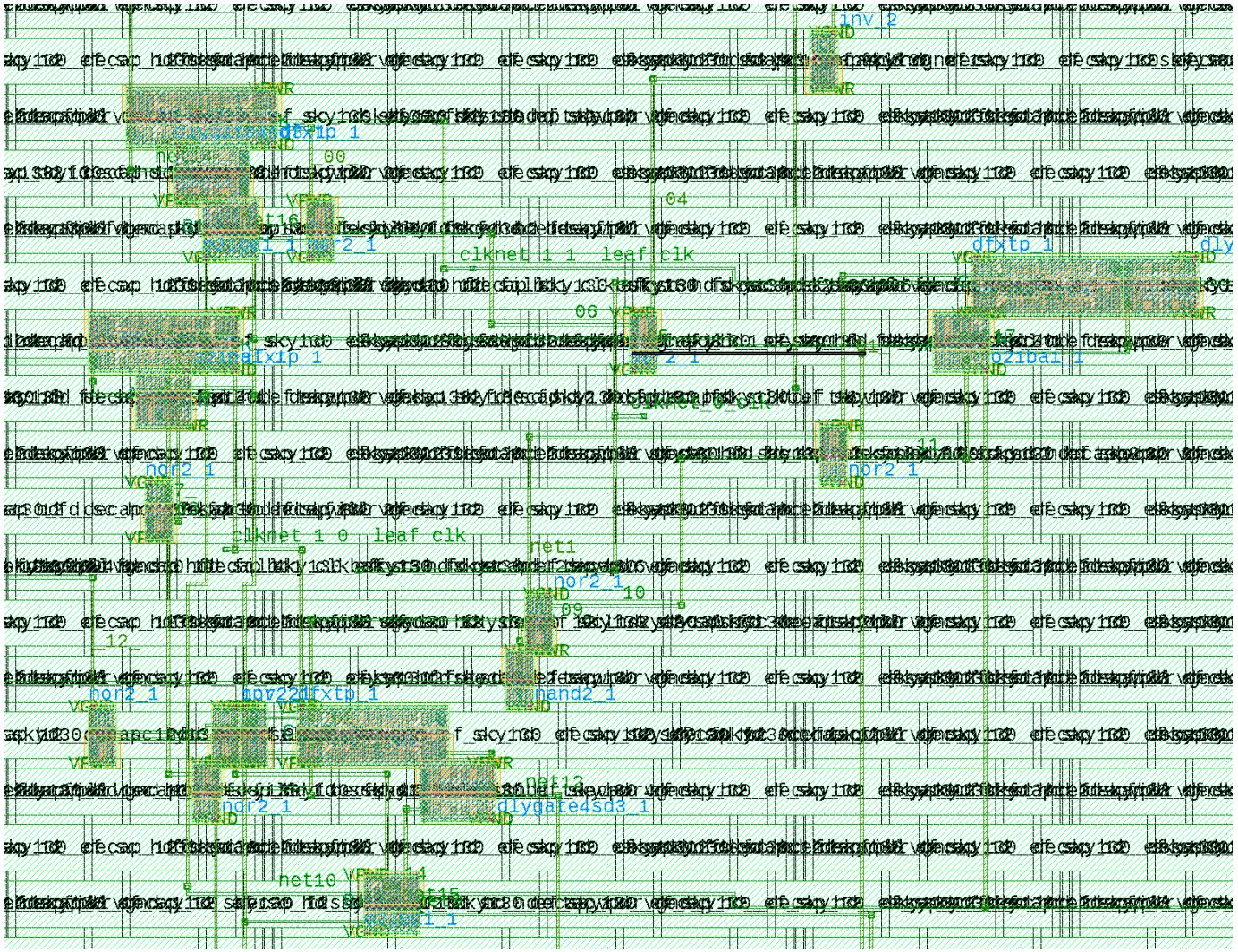
```
* NGSPICE file created from registeredNAND4.ext - technology: sky130A

* Black-box entry subcircuit for sky130_ef_sc_hd__decap_12 abstract view
.subckt sky130_ef_sc_hd__decap_12 VGND VNB VPB VPWR
.ends

* Black-box entry subcircuit for sky130_fd_sc_hd__tapvpwrvgnd_1 abstract view
.subckt sky130_fd_sc_hd__tapvpwrvgnd_1 VGND VPWR
.ends

* Black-box entry subcircuit for sky130_fd_sc_hd__decap_6 abstract view
.subckt sky130_fd_sc_hd__decap_6 VGND VNB VPB VPWR
.ends

* Black-box entry subcircuit for sky130_fd_sc_hd__fill_1 abstract view
.subckt sky130_fd_sc_hd__fill_1 VGND VNB VPB VPWR
.ends
```

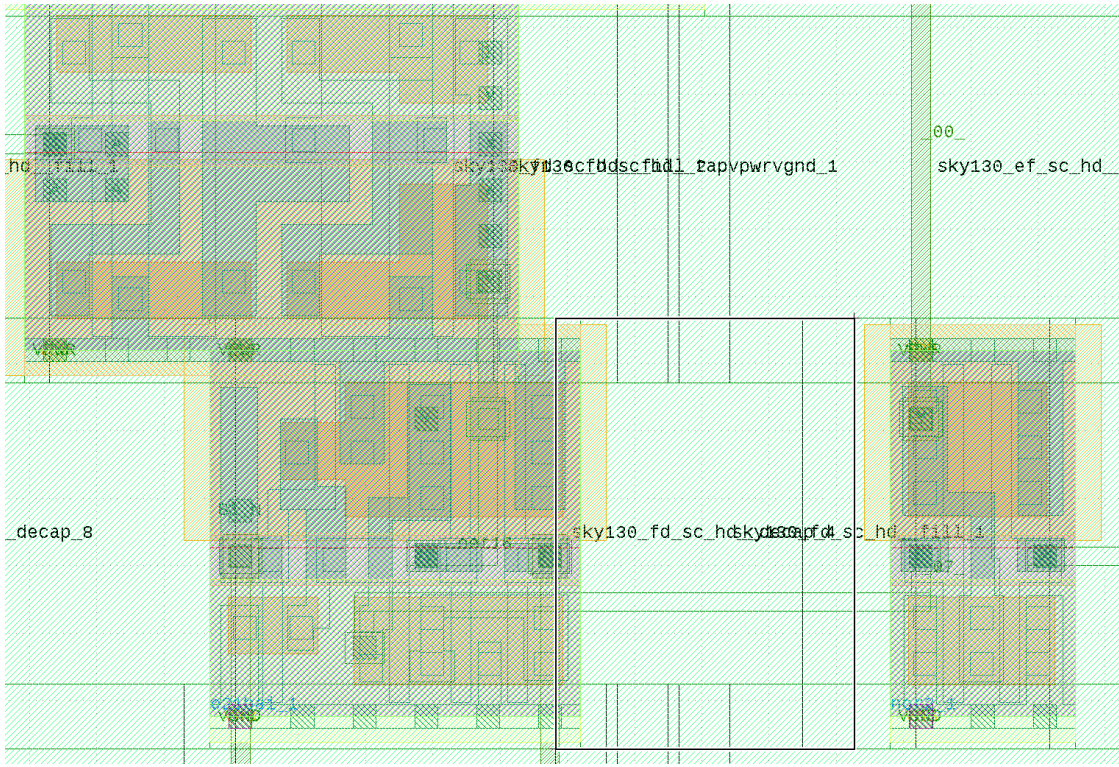
RC Extraction: Physical (shape) –> Electrical (R,C) (DEF -> Spice)

```
========================================================================
====================== Typical Corner ==================================

Startpoint: _39_ (rising edge-triggered flip-flop clocked by clk)
Endpoint: dout[2] (output port clocked by clk)
Path Group: clk
Path Type: max

Fanout     Cap    Slew   Delay    Time   Description
---------------------------------------------------------------------------
                          0.00    0.00   clock clk (rise edge)
                          0.00    0.00   clock source latency
                   0.12   0.08    0.08 ^ clk (in)
     1    0.02                           clk (net)
                   0.12   0.00    0.08 ^ clkbuf_0_clk/A (sky130_fd_sc_hd__clkbuf_16)
                   0.04   0.16    0.24 ^ clkbuf_0_clk/X (sky130_fd_sc_hd__clkbuf_16)
     2    0.02                           clknet_0_clk (net)
                   0.04   0.00    0.24 ^ clkbuf_1_0__f_clk/A (sky130_fd_sc_hd__clkbuf_16)
                   0.03   0.12    0.36 ^ clkbuf_1_0__f_clk/X (sky130_fd_sc_hd__clkbuf_16)
     2    0.01                           clknet_1_0__leaf_clk (net)
                   0.03   0.00    0.36 ^ _39_/CLK (sky130_fd_sc_hd__dfxtp_1)
                   0.23   0.45    0.81 ^ _39_/Q (sky130_fd_sc_hd__dfxtp_1)
     2    0.02                           net13 (net)
                   0.23   0.00    0.81 ^ output13/A (sky130_fd_sc_hd__clkbuf_4)
                   0.11   0.26    1.07 ^ output13/X (sky130_fd_sc_hd__clkbuf_4)
     1    0.03                           dout[2] (net)
                   0.11   0.00    1.07 ^ dout[2] (out)
                          0.00    1.07   data arrival time

                         10.00   10.00   clock clk (rise edge)
                          0.00   10.00   clock network delay (propagated)
                         -0.25    9.75   clock uncertainty
                          0.00    9.75   clock reconvergence pessimism
                         -2.00    7.75   output external delay
                          0.00    7.75   data required time
---------------------------------------------------------------------------
                          0.00    7.75   data required time
                         -0.00   -1.07   data arrival time
---------------------------------------------------------------------------
                          0.00    6.68   slack (MET)
```

```
========================================================================
 report_power
========================================================================
====================== Typical Corner ==================================

Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power (Watts)
----------------------------------------------------------------
Sequential             1.73e-05   1.79e-06   3.38e-11   1.91e-05  20.2%
Combinational          5.56e-05   1.97e-05   2.94e-09   7.53e-05  79.8%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------
Total                  7.30e-05   2.15e-05   2.98e-09   9.45e-05 100.0%
                          77.2%      22.7%       0.0%
```

GDSII Masks


clknet_1_1__leaf_clk
clknet_1_0__leaf_clk
dfxtp_1
nor2_1
nand2_1
dlygate4sd3_1


sky130_fd_sc_hd__decap_8
sky130_fd_sc_hd__fill_1

Nadzor nad tokom

```
set ::env(DESIGN_NAME) {erk_adder}
set ::env(VERILOG_FILES) [glob $::env(DESIGN_DIR)/src/*.v]
set ::env(CLOCK_PORT) "clk"
set ::env(CLOCK_PERIOD) "10.0"

set ::env(DESIGN_IS_CORE) {1}

set ::env(SYNTH_STRATEGY) {AREA 3}
#set ::env(SYNTH_ADDER_TYPE) {CSA}

# Set the core area and the placement density
# The core area is calculated from:
# FP_CORE_UTIL = (Area of standard cell instances used in design) / CORE AREA
# Hence, CORE AREA is set by setting the FP_CORE_UTIL :
# CORE AREA = (Area of standard cell instances used in design) / FP_CORE_UTIL
# As we have very tiny design, FP_CORE_UTIL should be very small in order to get CORE AREA large enough for power routing
# the placer will fill core area with fillers
set ::env(FP_CORE_UTIL) 1
set ::env(PL_TARGET_DENSITY) [ expr ($::env(FP_CORE_UTIL)+3) / 100.0 ]


# power lines : larger pitch requires larger core area - leave defaults for PDK
set ::env(FP_PDN_VPITCH) 153.6
set ::env(FP_PDN_HPITCH) 153.18
set ::env(FP_PDN_VOFFSET) 16.32
set ::env(FP_PDN_HOFFSET) 16.65


# Specifies the insertion strategy of diodes to be used in the flow. 0 = No diode insertion, 1 = Spray diodes, 2 = insert fake diodes and replace them with real diodes if needed.
#   3 = use FastRoute Antenna Avoidance flow, 4 = Use Sylvian's Custom Script for diode insertion on design pins and smartly inserting needed diodes inside the design,
#   5 = a mix of strategy 2 and 4. (Default: 3)
#set ::env(DIODE_INSERTION_STRATEGY) 3

set tech_specific_config "$::env(DESIGN_DIR)/$::env(PDK)_$::env(STD_CELL_LIBRARY)_config.tcl"
if { [file exists $tech_specific_config] == 1 } {
    source $tech_specific_config
}
```

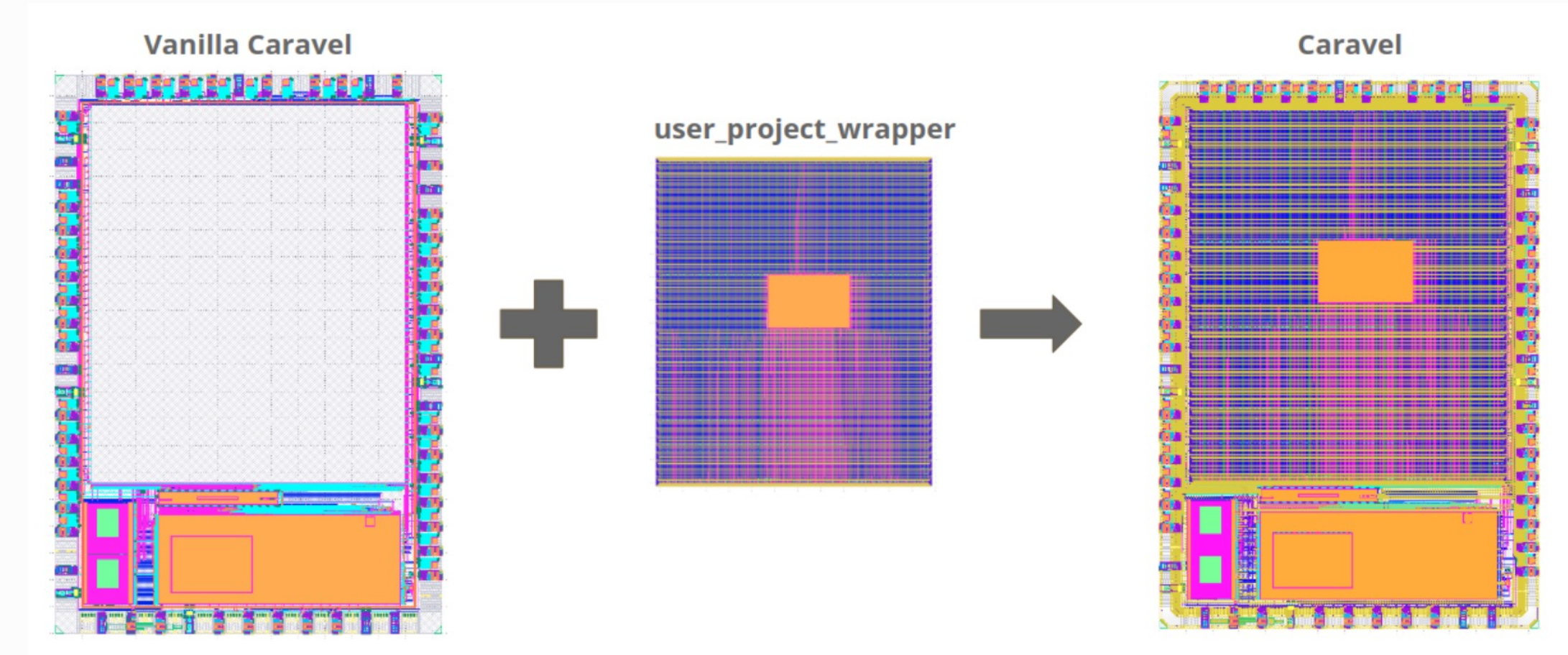
SYNTHESIS

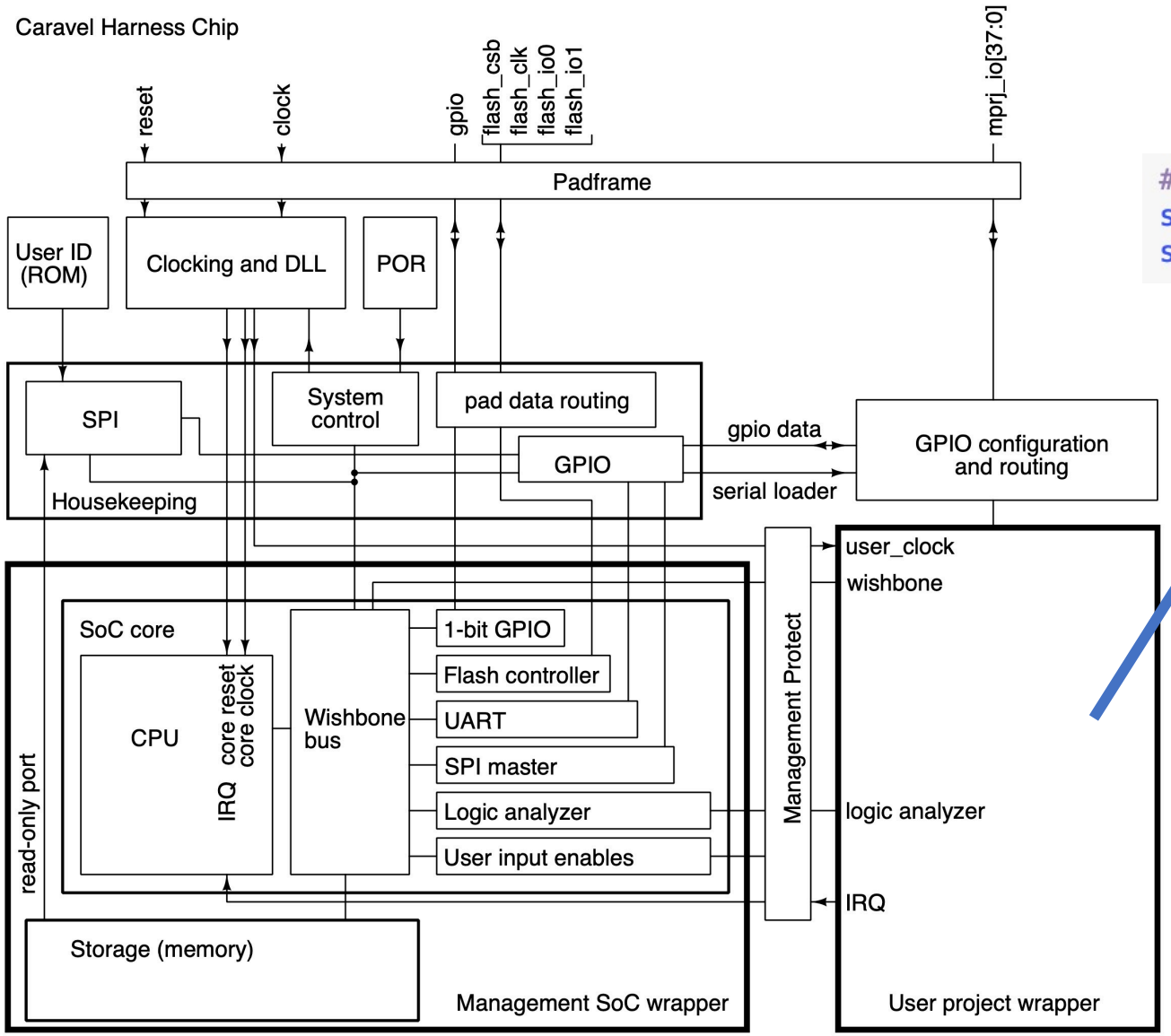
Strategy	Cells	Area (um^2)	Delay (ns)	Power (uW)	Area Ratio	Delay Ratio	Power Ratio
AREA 0	51	583.0592	3.32	18.4	1.00	1	1.00
AREA 3	73	724.4448	2.95	25.1	1.24	0.89	1.36
DELAY 2	68	708.1792	3.01	23.2	1.21	0.91	1.26
AREA 0/FP_UTIL	51	583.0592	3.32	18.4	1.00	1	1.00

P&R, PARASITIC EXTRACTION

Area (um^2)	Delay (ns)	Power (uW)	Area Ratio	Delay Ratio	Power Ratio
2092	3.84	65.2	1.00	1	1.00
2352	3.46	71.8	1.12	0.90	1.10
2427	1.08	67.9	1.16	0.28	1.04
971	3.54	45.1			

MPW Caravel






```
# Area Configurations. DON'T TOUCH.
set ::env(FP_SIZING) absolute
set ::env(DIE_AREA) "0 0 2920 3520"
```

User Project Area

This is the user space. It has a limited silicon area `2.92mm x 3.52mm` as well as a fixed number of I/O pads `38` and power pads `4`.