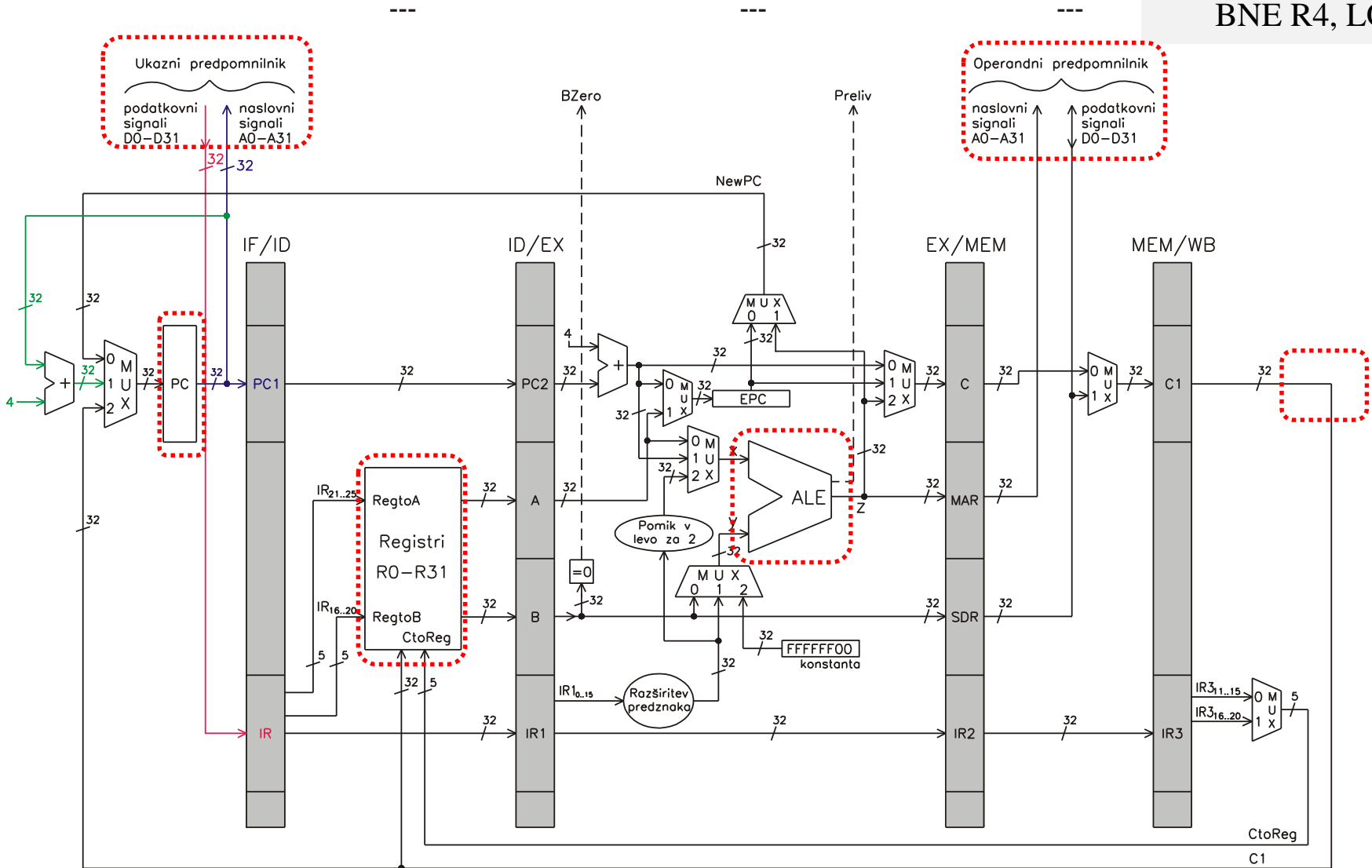


# HIP – shema cevododa brez premostitev

Program:  
 LOOP: LW R1,0(R2)  
 ADDI R1,R1,#1  
 SW 0(R2),R1  
 SUB R4,R3,R2  
 BNE R4, LOOP

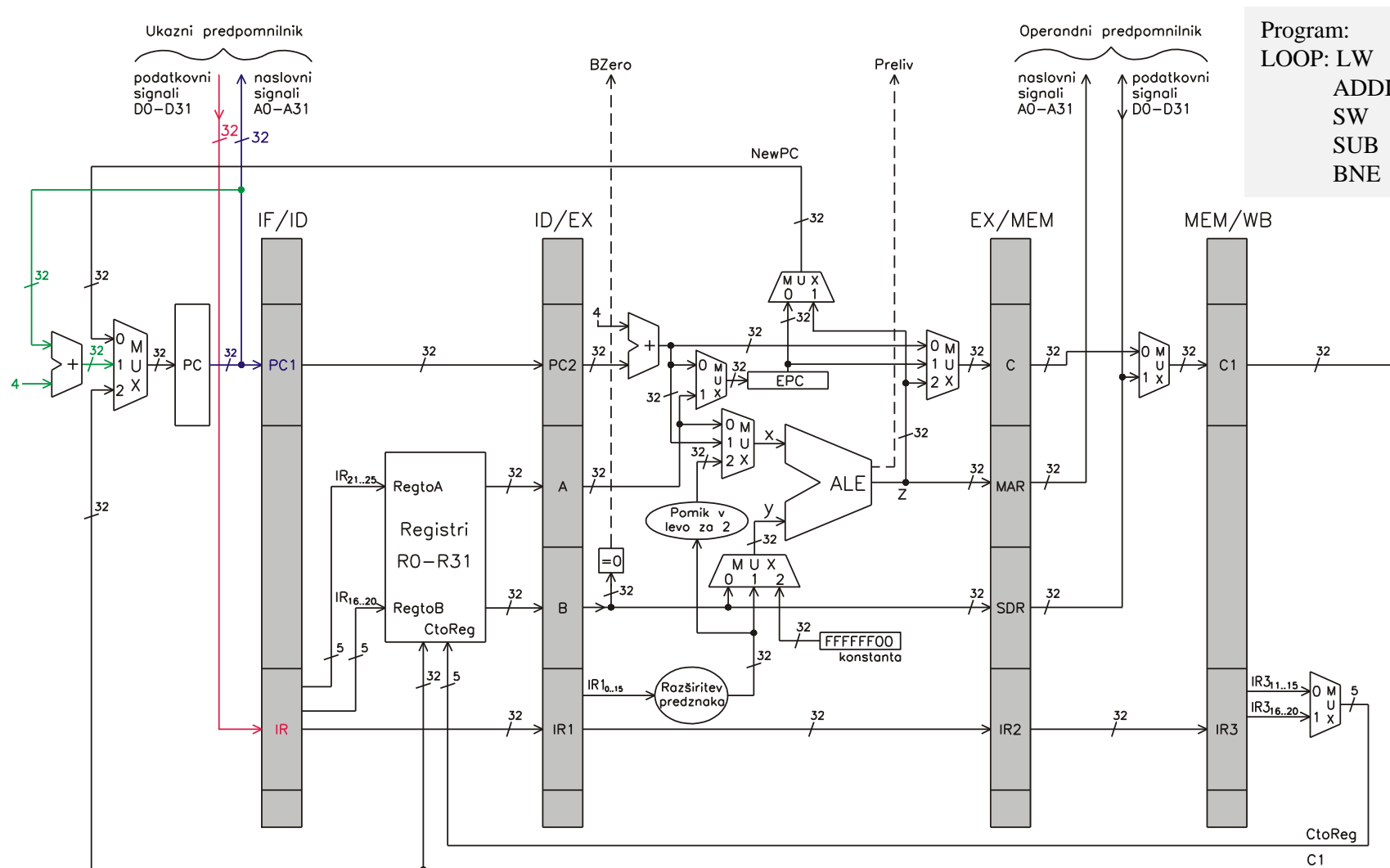


# Perioda 1

LW R1,0(R2)

# HIP - brez premostitev

BNE R4,LOOP



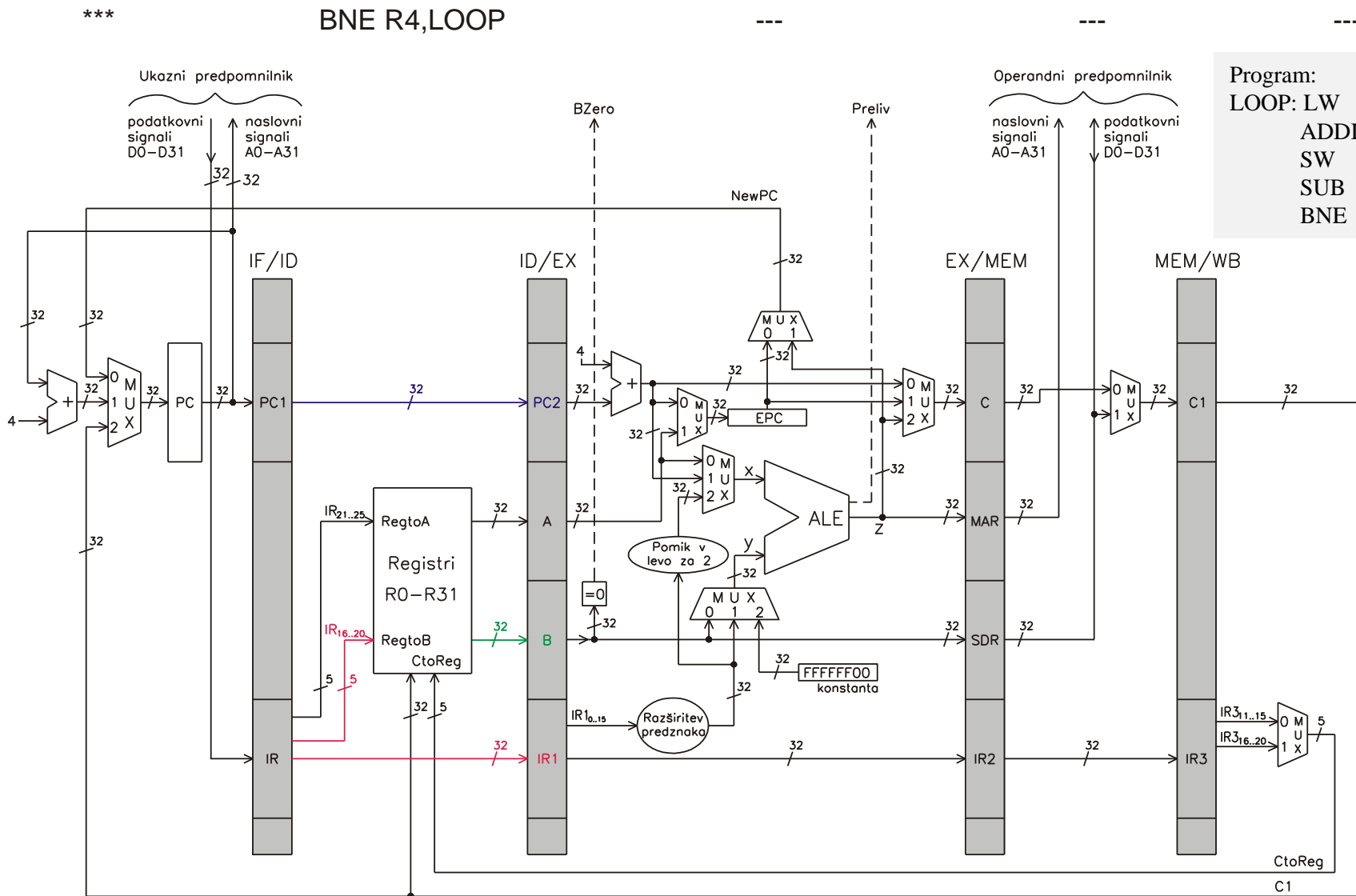
```

Program:
LOOP: LW    R1, 0(R2)
      ADDI  R1, R1, #1
      SW    0(R2),R1
      SUB   R4, R3, R2
      BNE  R4, LOOP
    
```

# Perioda 2

LW R1,0(R2)

# HIP - brez premostitev



Program:

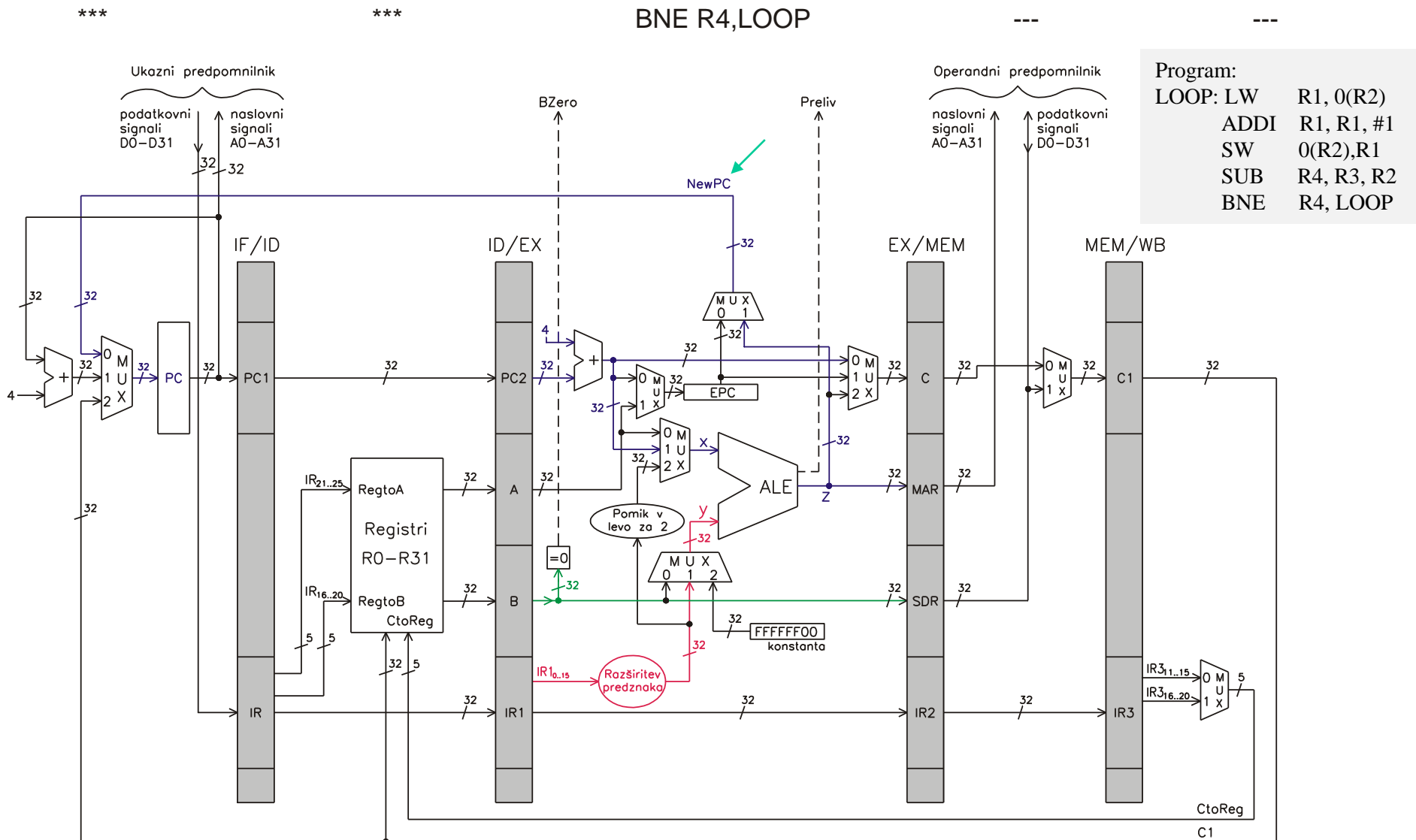
```

LOOP: LW    R1, 0(R2)
      ADDI  R1, R1, #1
      SW    0(R2), R1
      SUB   R4, R3, R2
      BNE  R4, LOOP
    
```

# Perioda 3

LW R1,0(R2)

# HIP - brez premostitev



# Perioda 4

# HIP - brez premostitev

ADDI R1,R1,#1

LW R1,0(R2)

\*\*\*

\*\*\*

BNE R4,LOOP

---

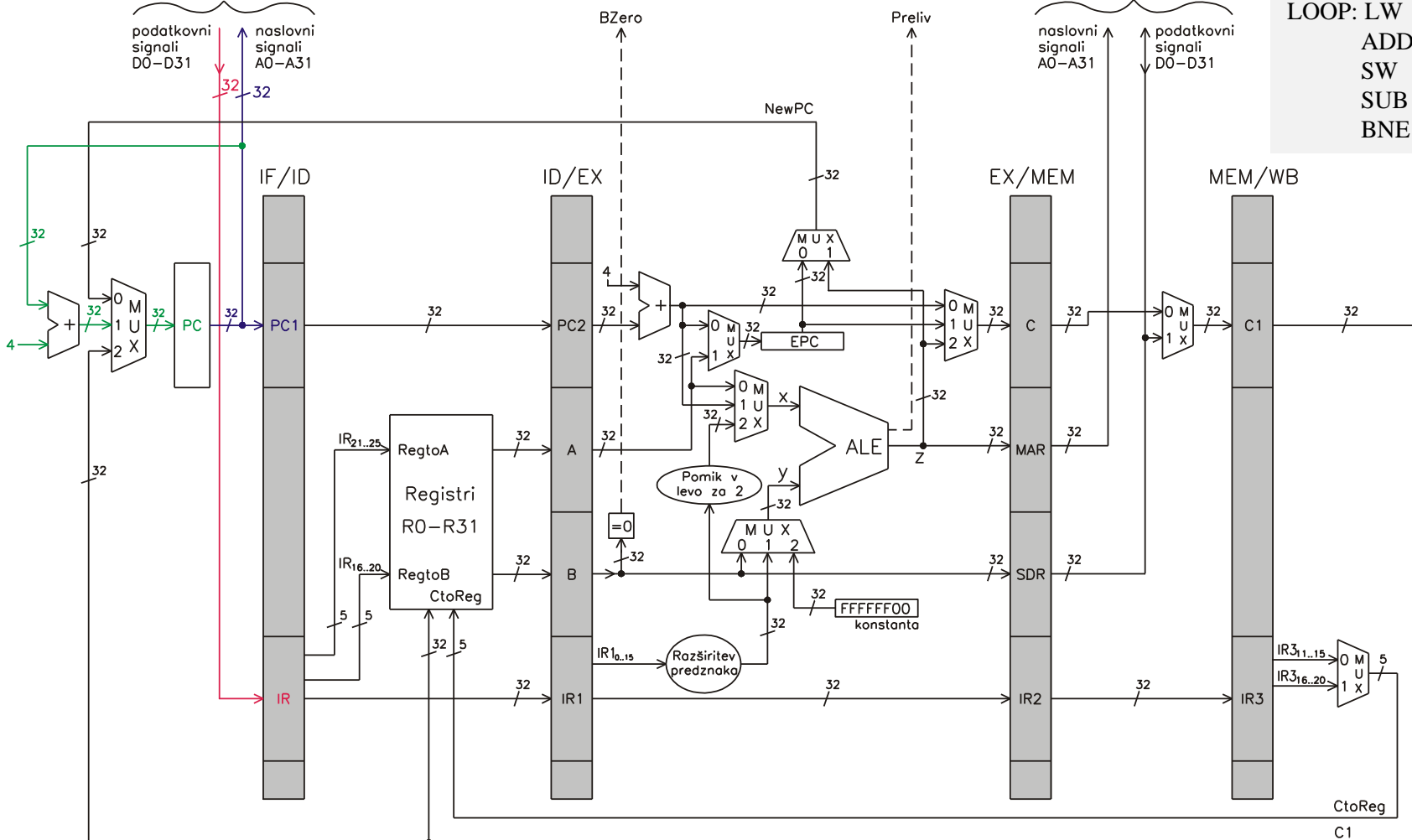
Ukazni predpomnilnik

podatkovni signali D0-D31  
naslovni signali A0-A31

Operandni predpomnilnik

naslovni signali A0-A31  
podatkovni signali D0-D31

Program:  
 LOOP: LW R1, 0(R2)  
 ADDI R1, R1, #1  
 SW 0(R2),R1  
 SUB R4, R3, R2  
 BNE R4, LOOP



# Perioda 5

# HIP - brez premostitev

ADDI R1,R1,#1

LW R1,0(R2)

\*\*\*

\*\*\*

BNE R4,LOOP

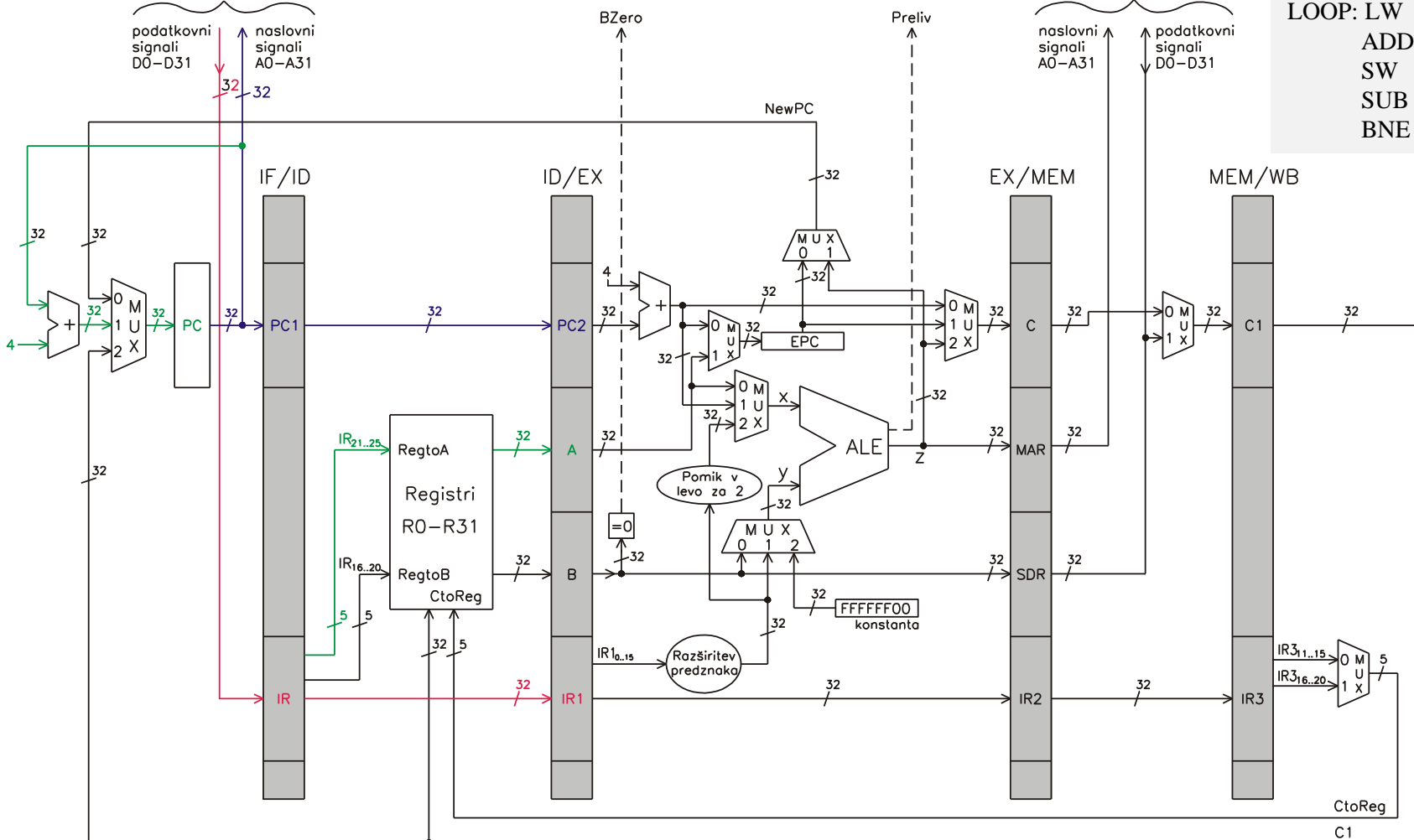
Ukazni predpomnilnik

podatkovni signali D0-D31  
naslovni signali A0-A31

Operandni predpomnilnik

naslovni signali A0-A31  
podatkovni signali D0-D31

Program:  
 LOOP: LW R1, 0(R2)  
 ADDI R1, R1, #1  
 SW 0(R2),R1  
 SUB R4, R3, R2  
 BNE R4, LOOP



# Perioda 6

# HIP - brez premostitev

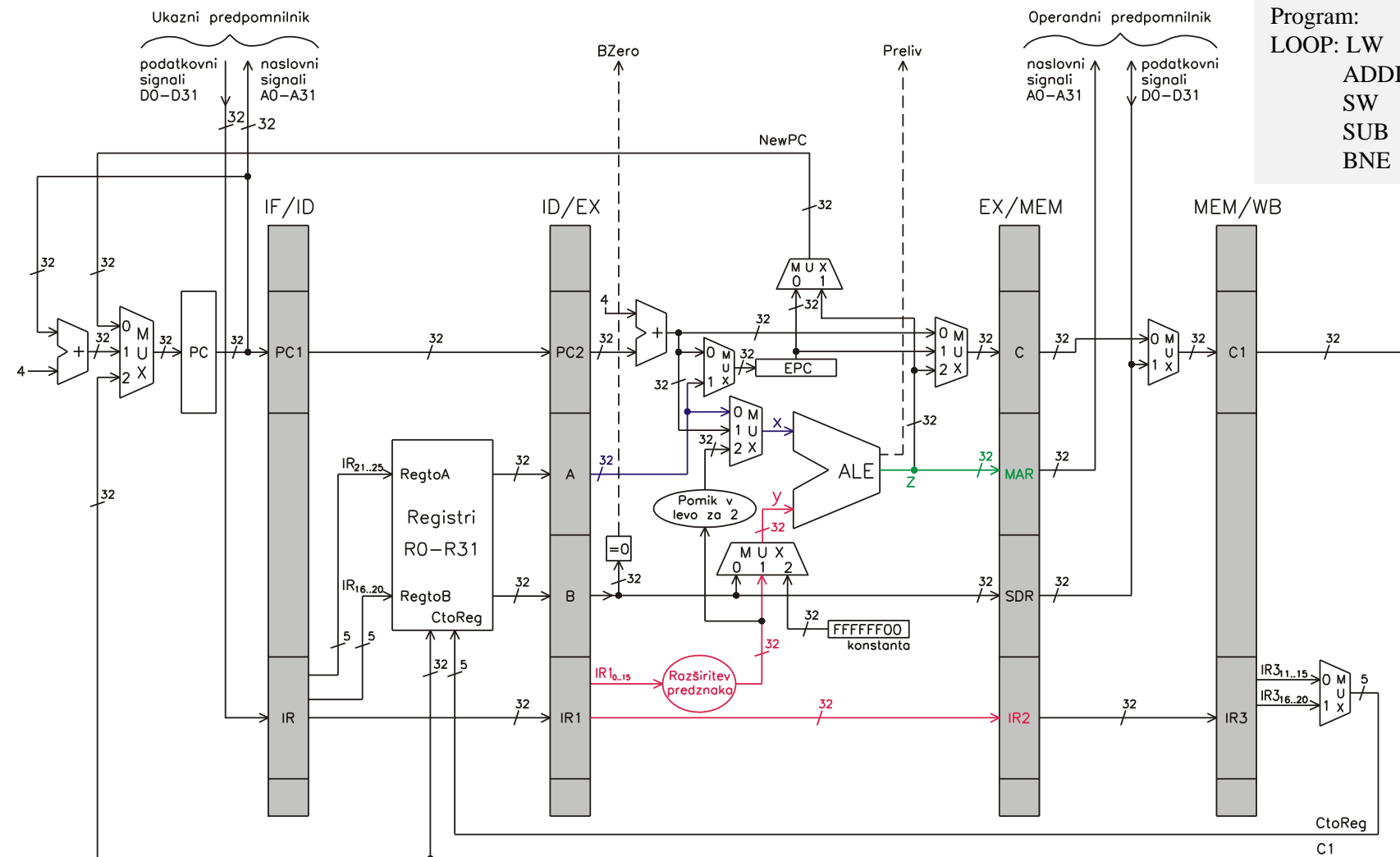
ADDI R1,R1,#1

\*\*\*

LW R1,0(R2)

\*\*\*

\*\*\*



```

Program:
LOOP: LW   R1, 0(R2)
      ADDI R1, R1, #1
      SW   0(R2),R1
      SUB  R4, R3, R2
      BNE R4, LOOP
    
```

# Perioda 7

# HIP - brez premostitev

ADDI R1,R1,#1

\*\*\*

\*\*\*

LW R1,0(R2)

\*\*\*

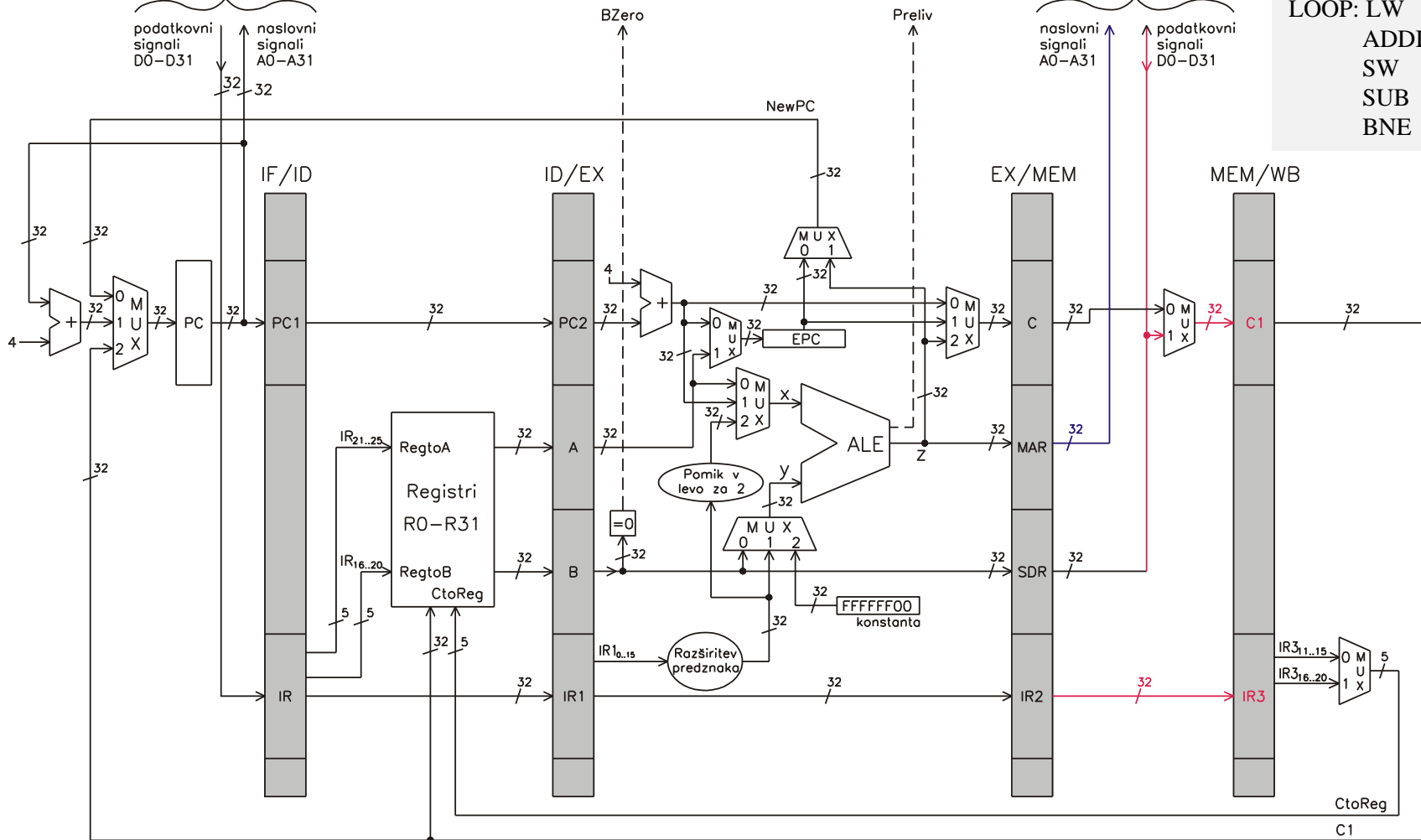
Ukazni predpomnilnik

podatkovni signali D0-D31  
naslovni signali A0-A31

Operandni predpomnilnik

naslovni signali A0-A31  
podatkovni signali D0-D31

Program:  
 LOOP: LW R1, 0(R2)  
 ADDI R1, R1, #1  
 SW 0(R2),R1  
 SUB R4, R3, R2  
 BNE R4, LOOP





# Perioda 8

SW 0(R2),R1

# HIP - brez premostitev

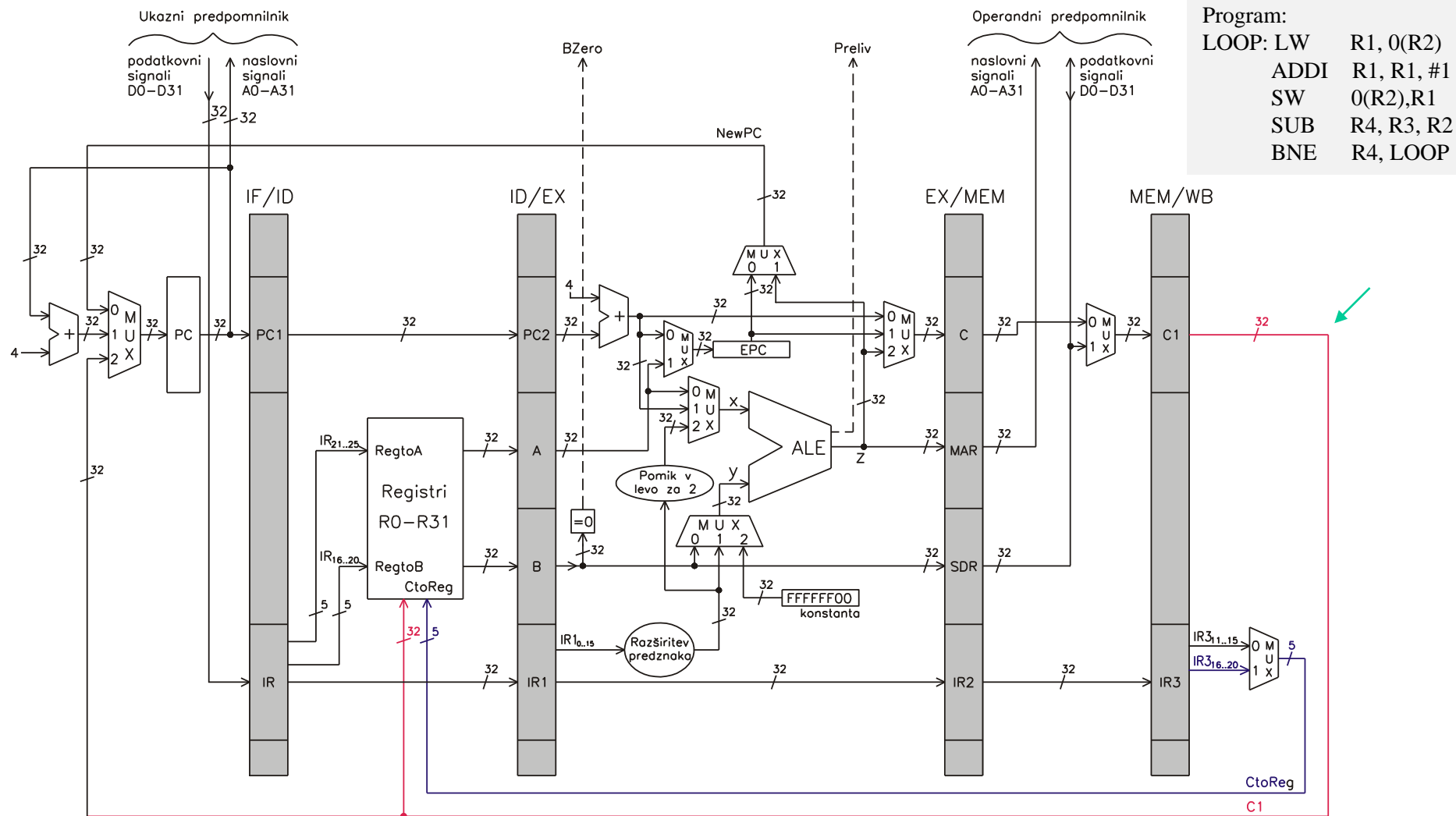
ADDI R1,R1,#1

\*\*\*

\*\*\*

\*\*\*

LW R1,0(R2)



```

Program:
LOOP: LW   R1, 0(R2)
      ADDI R1, R1, #1
      SW   0(R2),R1
      SUB  R4, R3, R2
      BNE R4, LOOP
    
```

# Perioda 9

# HIP - brez premostitev

SW 0(R2),R1

ADDI R1,R1,#1

\*\*\*

\*\*\*

\*\*\*

Ukazni predpomnilnik

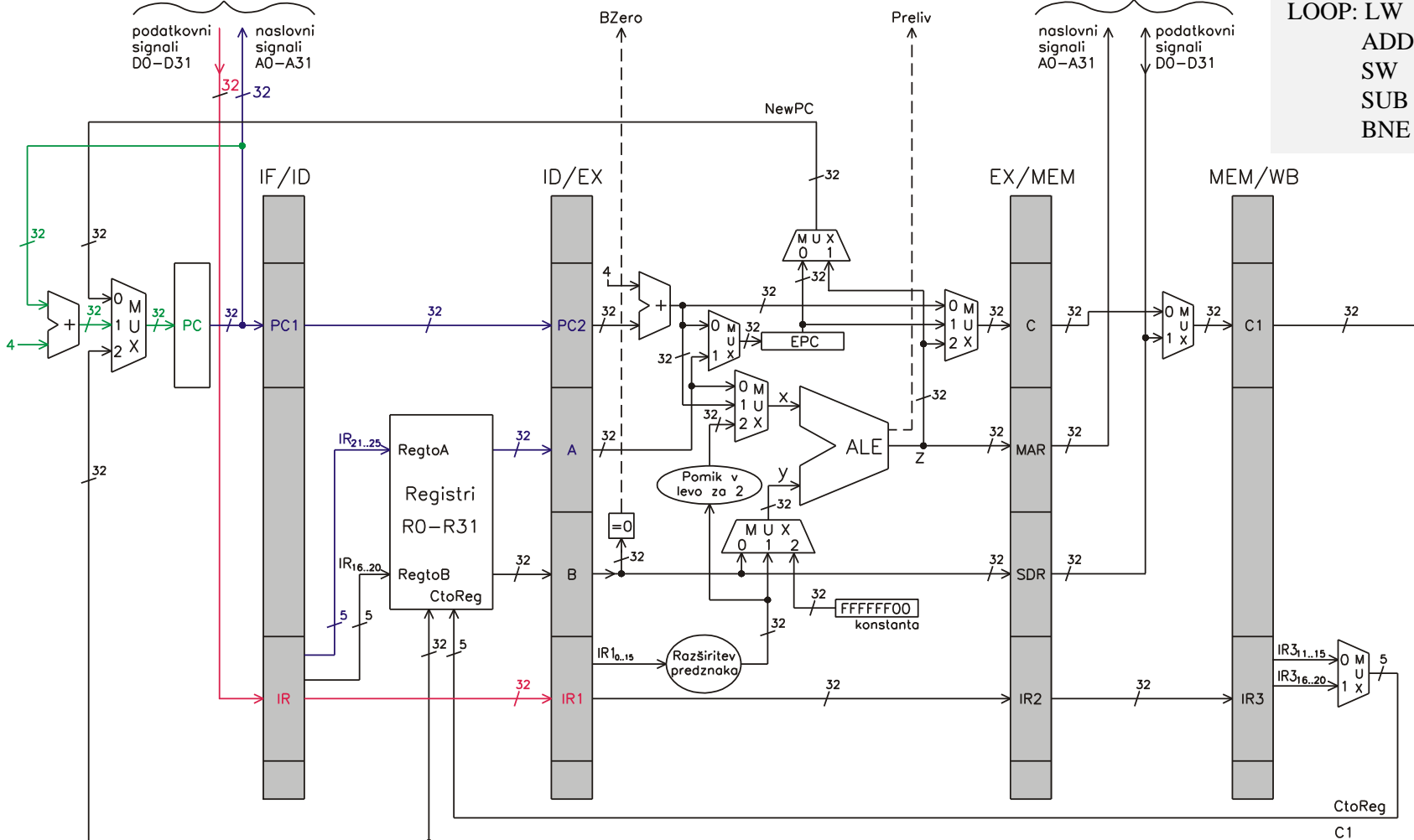
podatkovni signali D0-D31  
naslovni signali A0-A31

Operandni predpomnilnik

naslovni signali A0-A31  
podatkovni signali D0-D31

```

Program:
LOOP: LW    R1, 0(R2)
      ADDI  R1, R1, #1
      SW    0(R2),R1
      SUB   R4, R3, R2
      BNE  R4, LOOP
    
```



# Perioda 10

# HIP - brez premostitev

SW 0(R2),R1

\*\*\*

ADDI R1,R1,#1

\*\*\*

\*\*\*

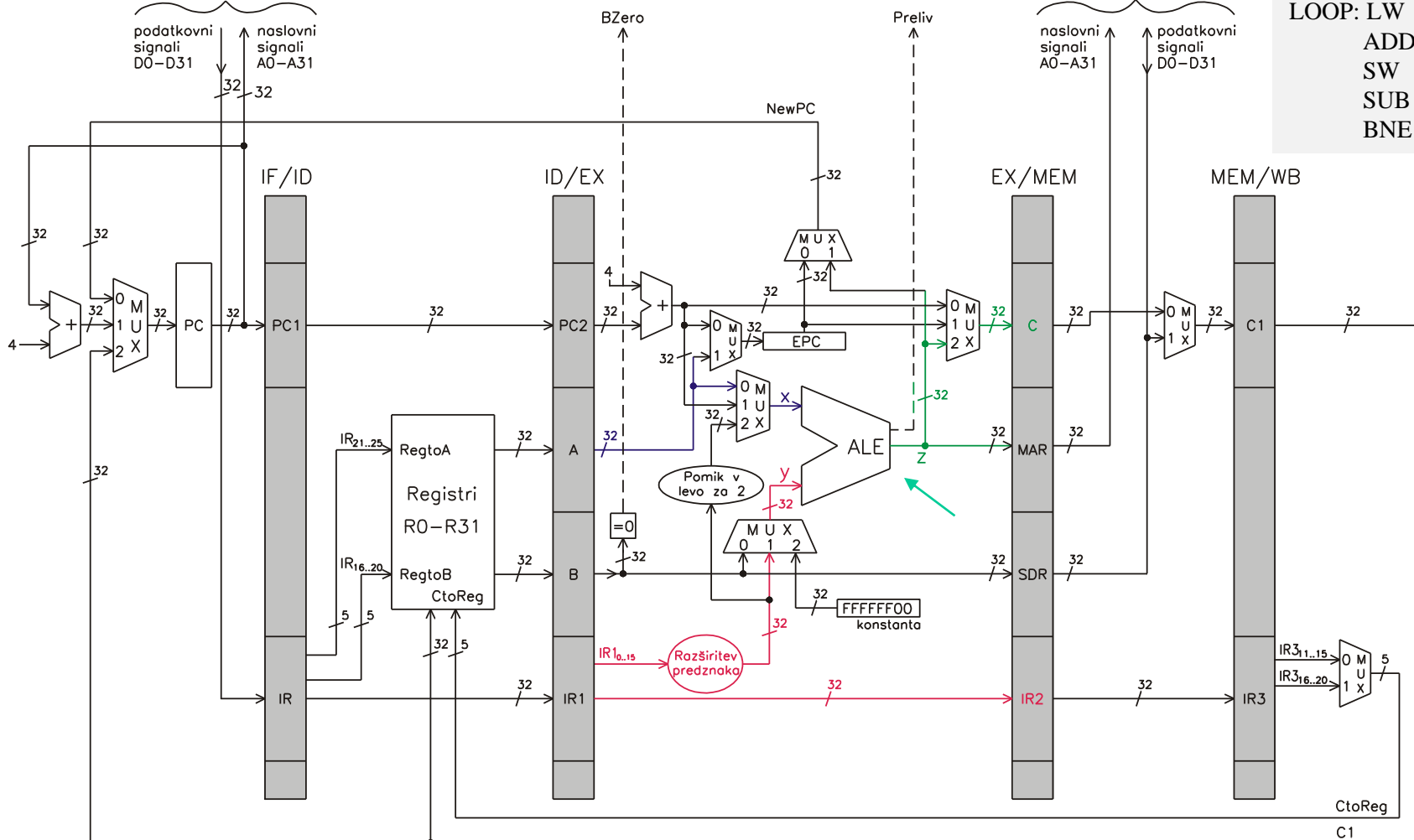
Ukazni predpomnilnik

podatkovni signali D0-D31  
naslovni signali A0-A31

Operandni predpomnilnik

naslovni signali A0-A31  
podatkovni signali D0-D31

Program:  
 LOOP: LW R1, 0(R2)  
 ADDI R1, R1, #1  
 SW 0(R2),R1  
 SUB R4, R3, R2  
 BNE R4, LOOP



# Perioda 11

# HIP - brez premostitev

SW 0(R2),R1

\*\*\*

\*\*\*

ADDI R1,R1,#1

\*\*\*

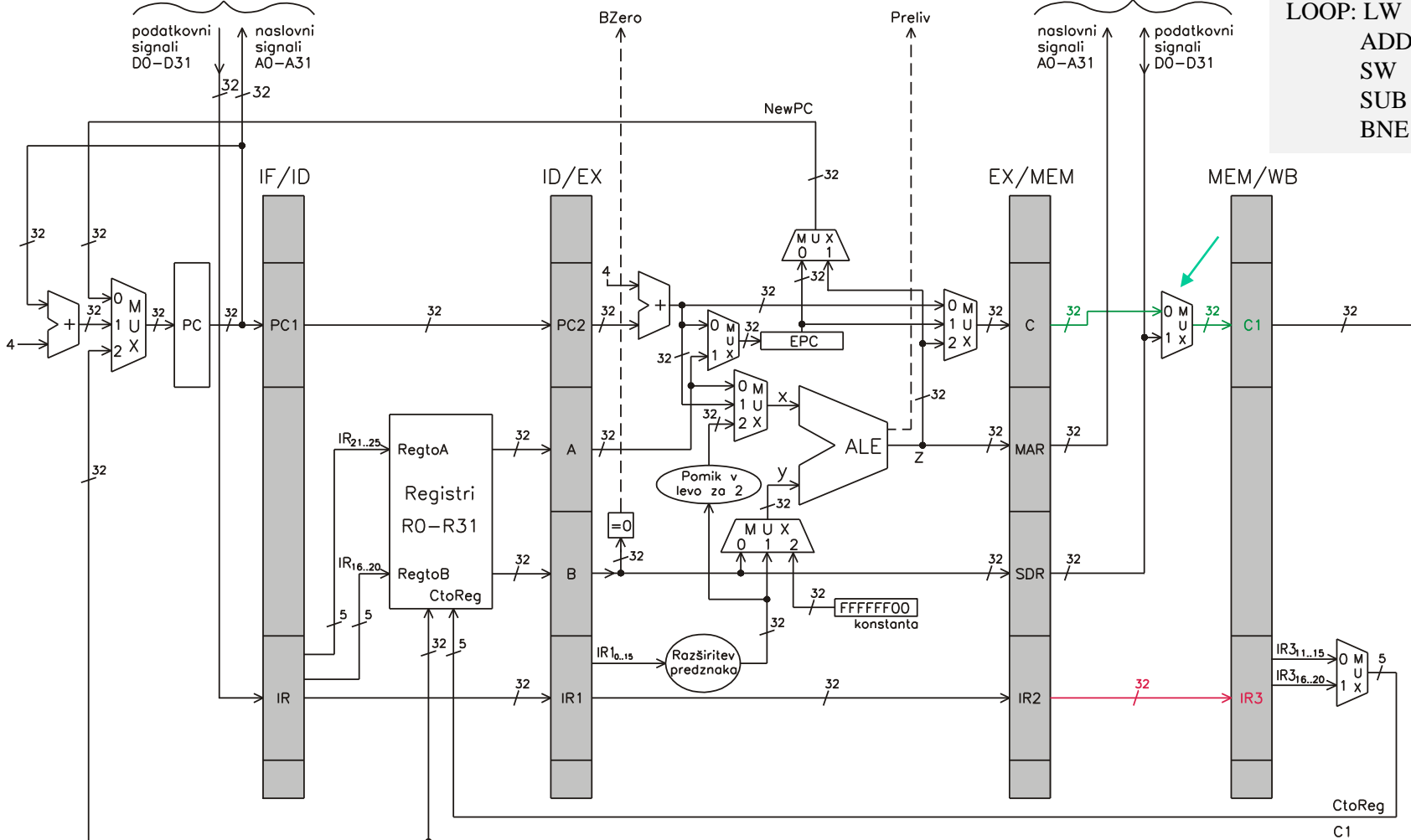
Ukazni predpomnilnik

podatkovni signali D0-D31  
naslovni signali A0-A31

Operandni predpomnilnik

naslovni signali A0-A31  
podatkovni signali D0-D31

Program:  
 LOOP: LW R1, 0(R2)  
 ADDI R1, R1, #1  
 SW 0(R2),R1  
 SUB R4, R3, R2  
 BNE R4, LOOP



CtoReg  
C1

# Perioda 12

# HIP - brez premostitev

SUB R4,R3,R2

SW 0(R2),R1

\*\*\*

\*\*\*

\*\*\*

ADDI R1,R1,#1

Ukazni predpomnilnik

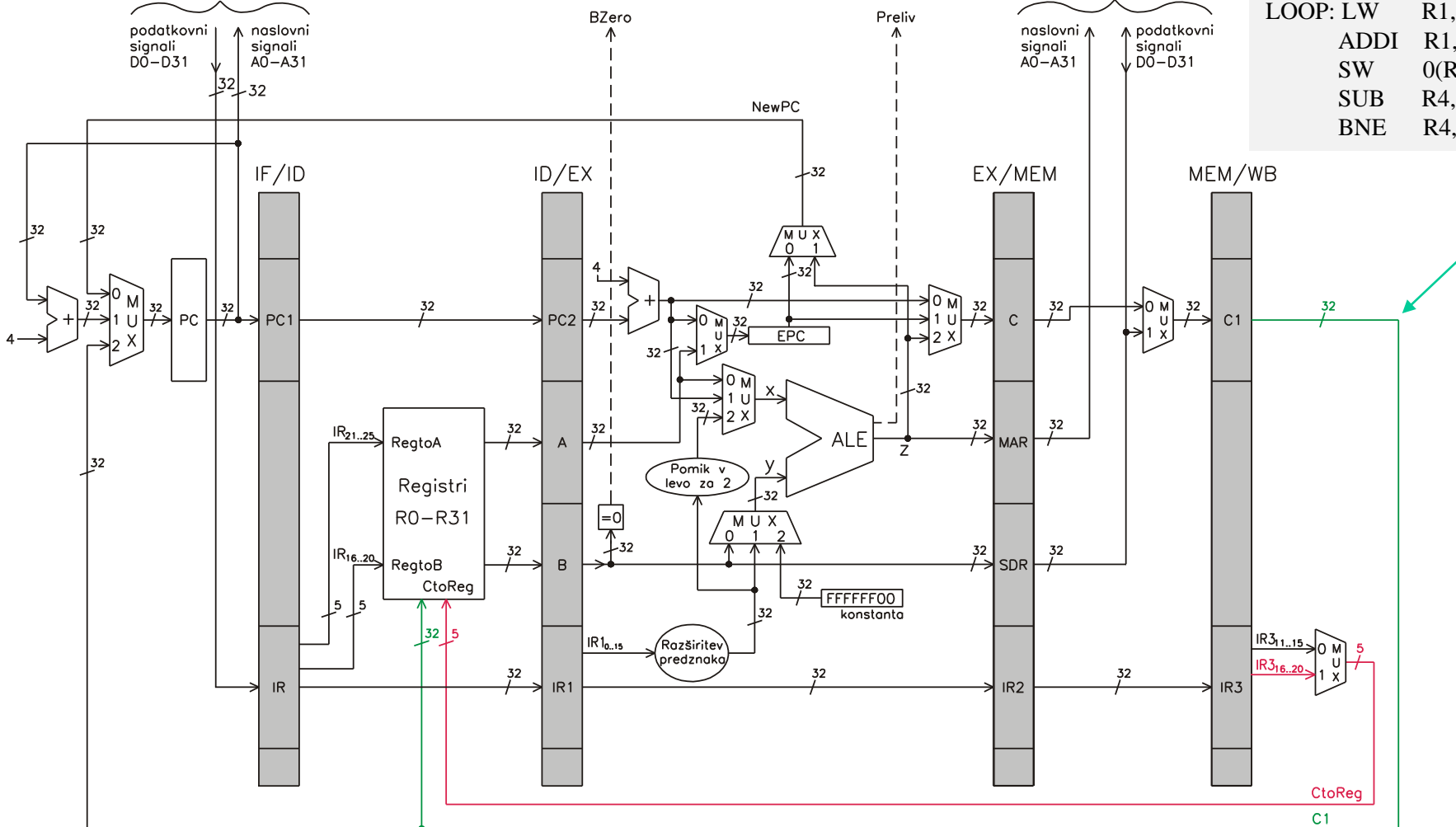
podatkovni signali D0-D31  
naslovni signali A0-A31

Operandni predpomnilnik

naslovni signali A0-A31  
podatkovni signali D0-D31

```

Program:
LOOP: LW    R1, 0(R2)
      ADDI  R1, R1, #1
      SW    0(R2),R1
      SUB   R4, R3, R2
      BNE  R4, LOOP
    
```



CtoReg  
C1

# Perioda 13

# HIP - brez premostitev

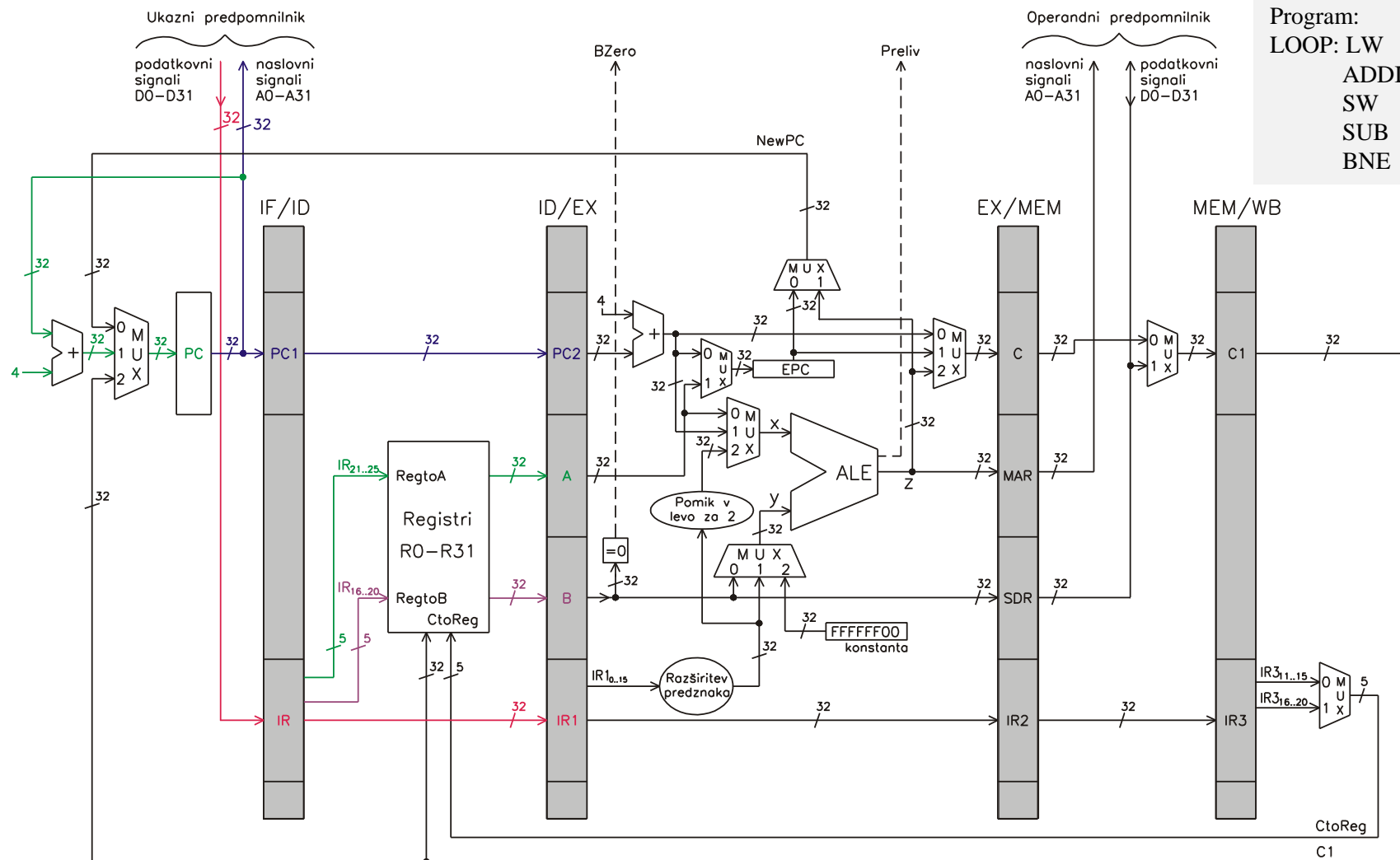
SUB R4,R3,R2

SW 0(R2),R1

\*\*\*

\*\*\*

\*\*\*



Program:  
 LOOP: LW R1, 0(R2)  
 ADDI R1, R1, #1  
 SW 0(R2),R1  
 SUB R4, R3, R2  
 BNE R4, LOOP

# Perioda 14

# HIP - brez premostitev

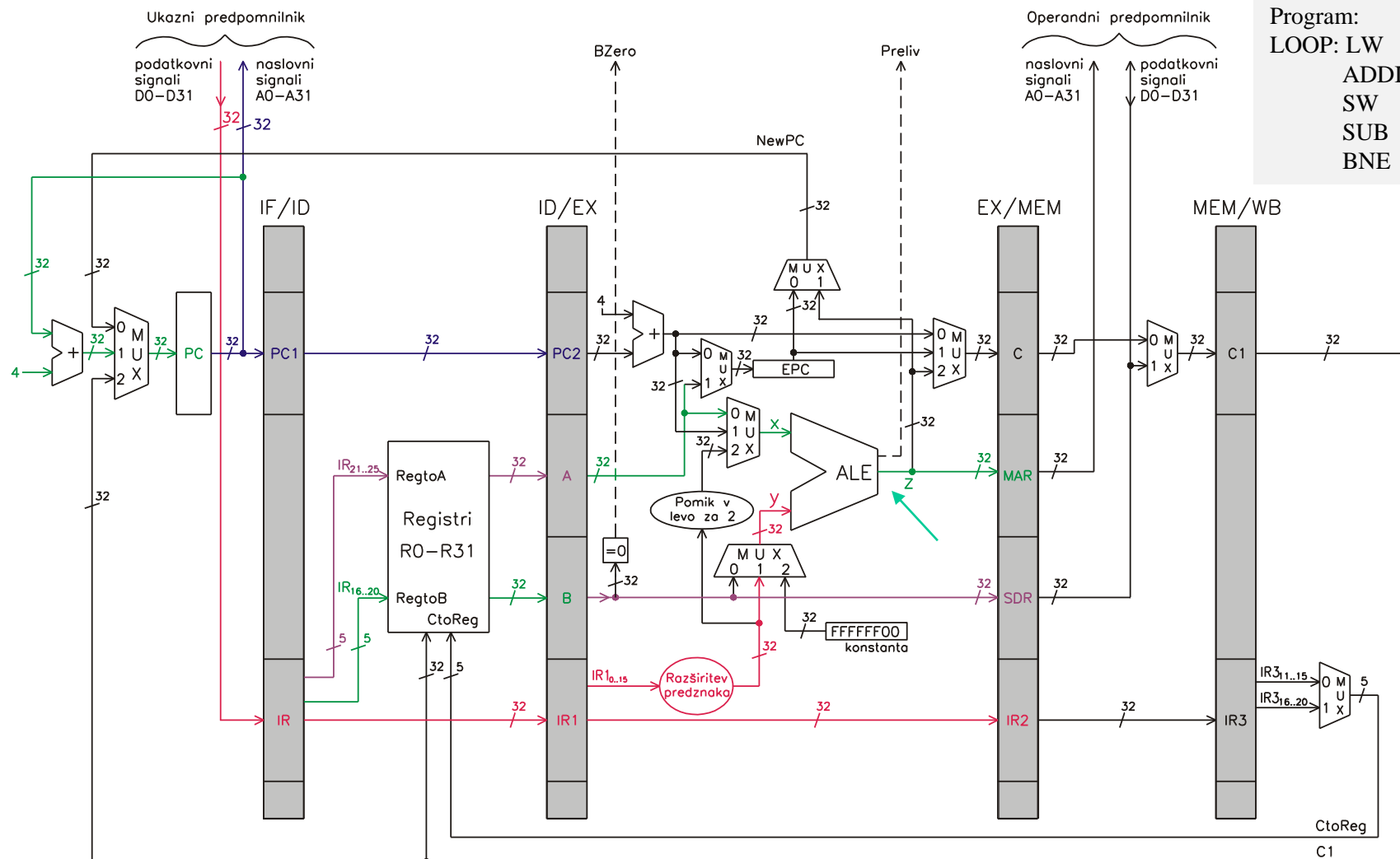
BNE R4,LOOP

SUB R4,R3,R2

SW 0(R2),R1

\*\*\*

\*\*\*



```

Program:
LOOP: LW    R1, 0(R2)
      ADDI  R1, R1, #1
      SW    0(R2),R1
      SUB   R4, R3, R2
      BNE  R4, LOOP
    
```

# Perioda 15

# HIP - brez premostitev

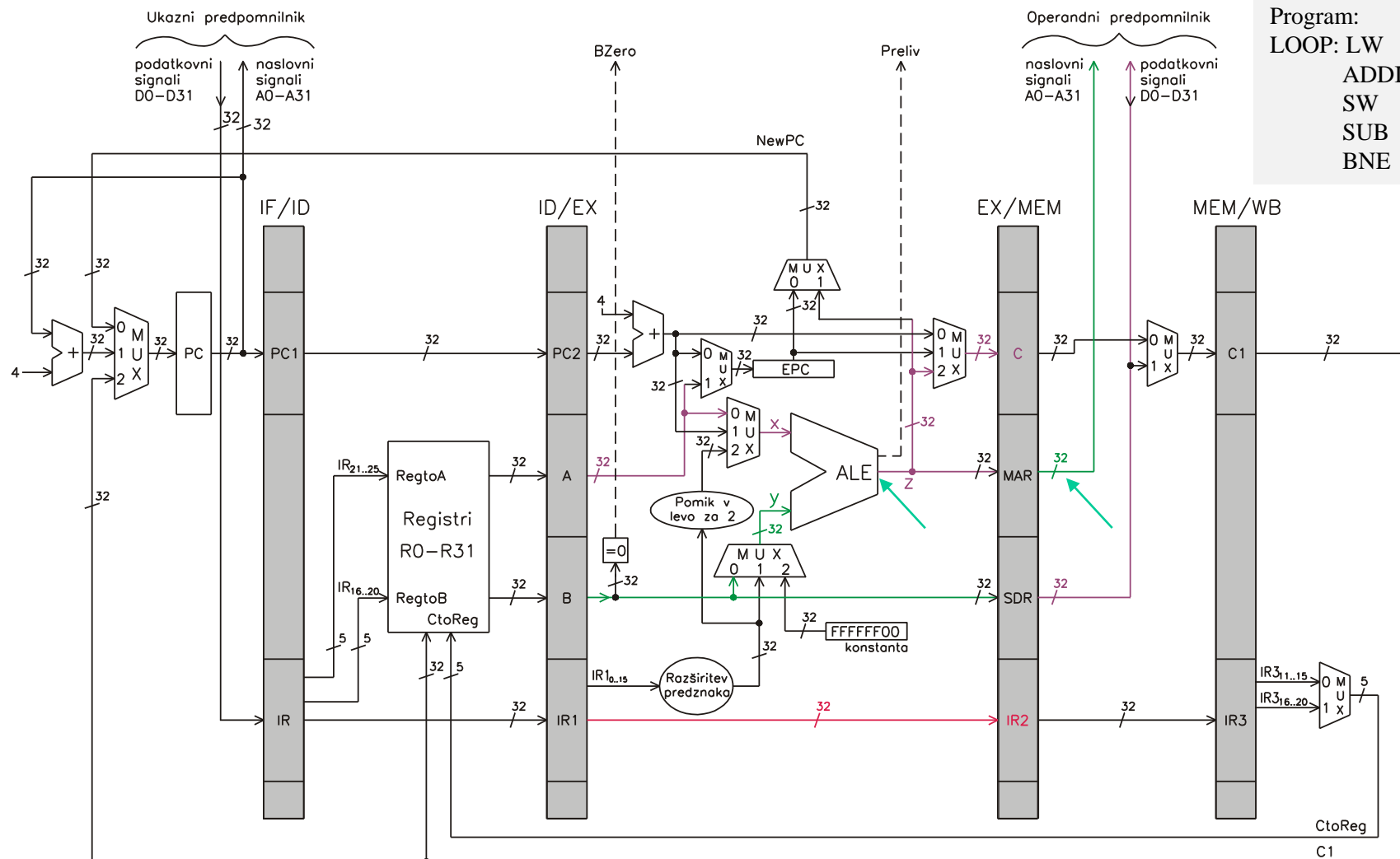
BNE R4,LOOP

\*\*\*

SUB R4,R3,R2

SW 0(R2),R1

\*\*\*



```

Program:
LOOP: LW    R1, 0(R2)
      ADDI  R1, R1, #1
      SW    0(R2),R1
      SUB   R4, R3, R2
      BNE  R4, LOOP
    
```



# Perioda 16

# HIP - brez premostitev

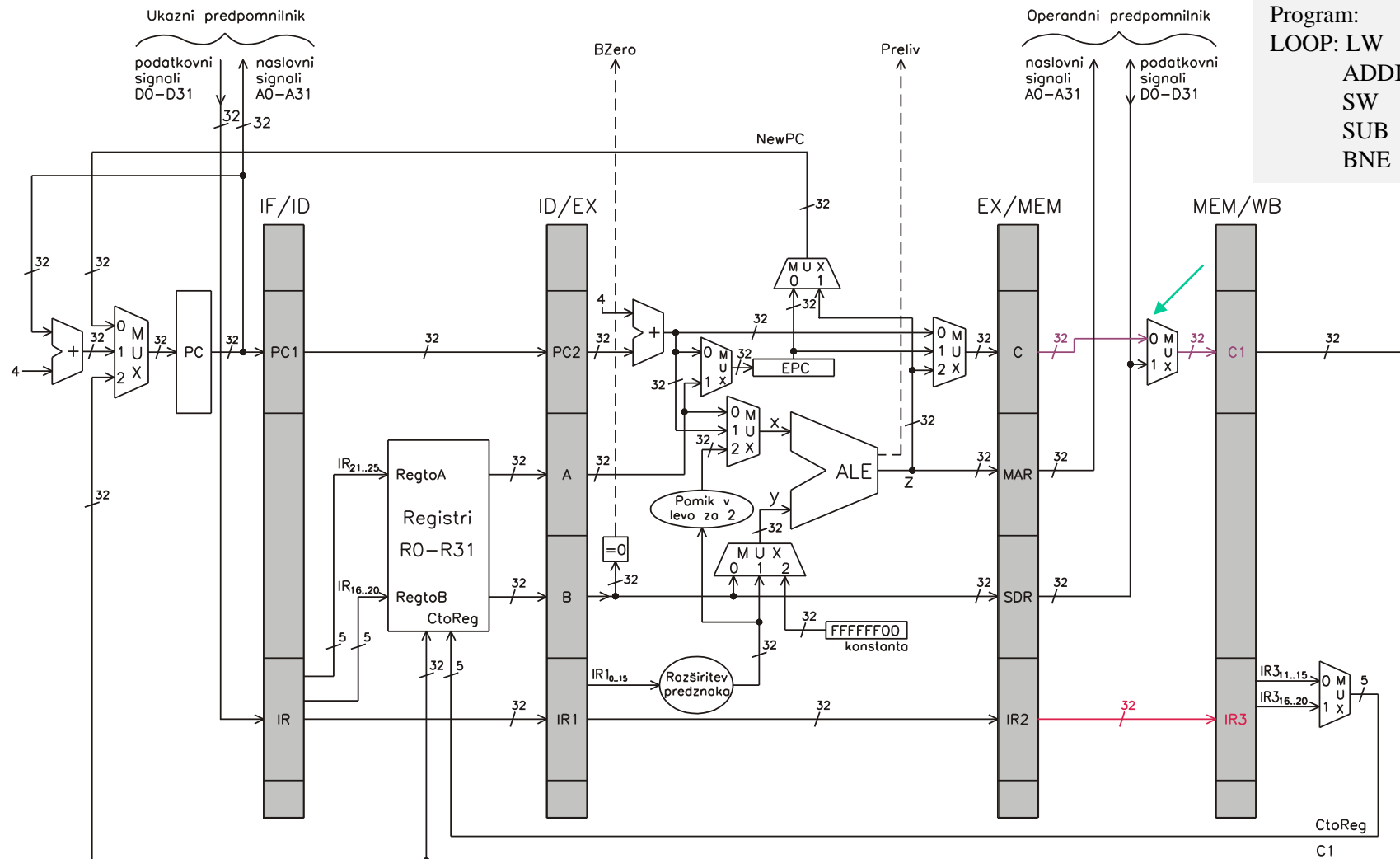
BNE R4,LOOP

\*\*\*

\*\*\*

SUB R4,R3,R2

SW 0(R2),R1



Program:

```

LOOP: LW    R1, 0(R2)
      ADDI  R1, R1, #1
      SW    0(R2),R1
      SUB   R4, R3, R2
      BNE  R4, LOOP
    
```

# Perioda 17

# HIP - brez premostitev

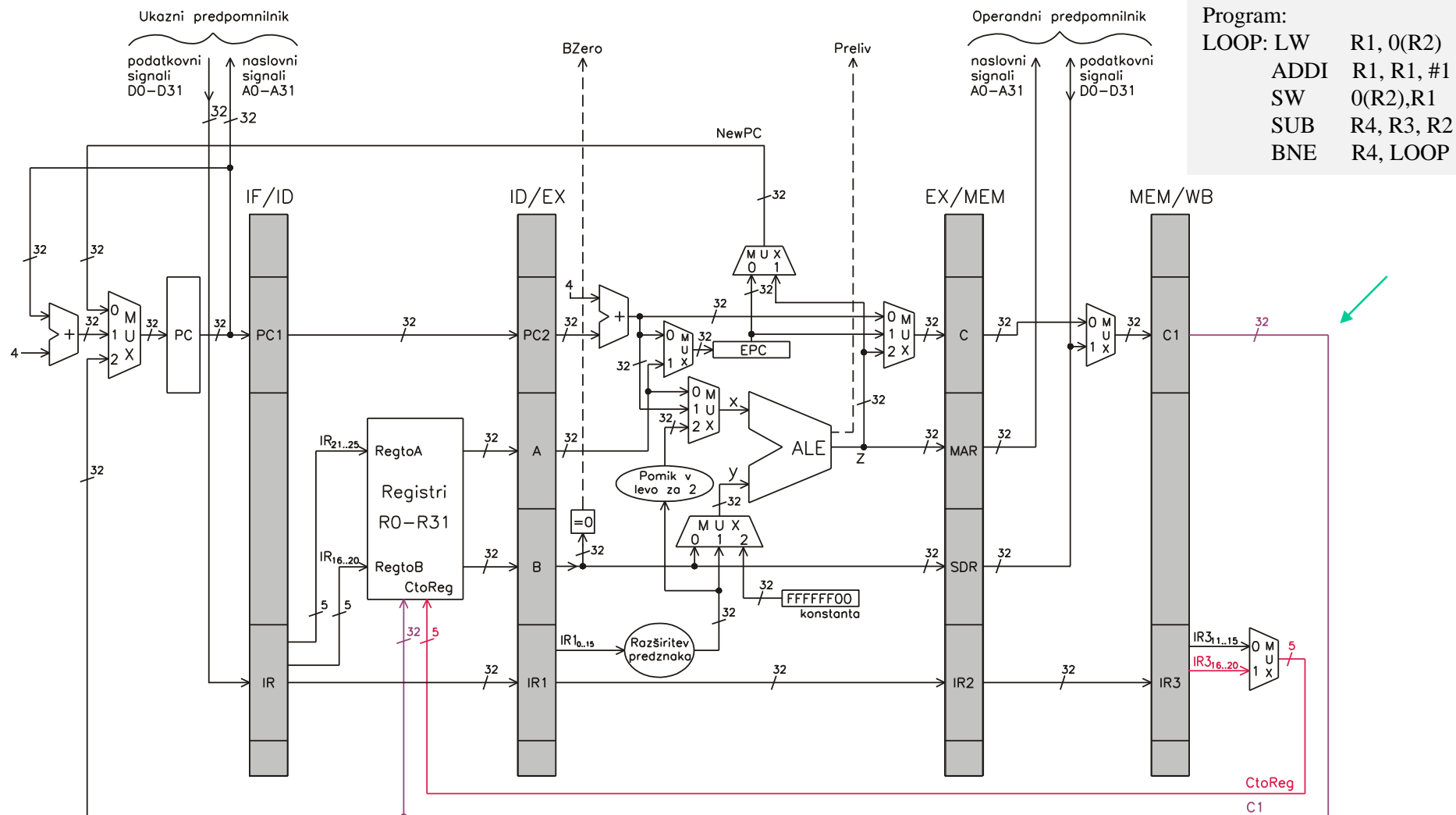
BNE R4,LOOP

\*\*\*

\*\*\*

\*\*\*

SUB R4,R3,R2



# Perioda 18

# HIP - brez premostitev

\*\*\* BNE R4,LOOP \*\*\*

Program:  
 LOOP: LW R1, 0(R2)  
 ADDI R1, R1, #1  
 SW 0(R2),R1  
 SUB R4, R3, R2  
 BNE R4, LOOP

