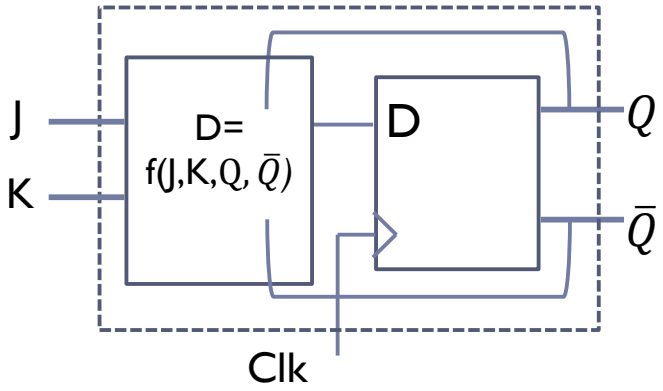
Digitalna vezja
UL, FRI

Vaja 14 Pomnilna celica JK

- Realizirajte sinhronsko pomnilno celico JK, če imate na voljo sinhronsko pomnilno celico D in logična vrata NOT in 2/1 MUX.

1. **Blok shema** logičnega vezja



2. Karakteristična tabela delovanja pomnilne celice D in JK.

D	$Q(t+1)$
0	0
1	1

J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$\overline{Q(t)}$

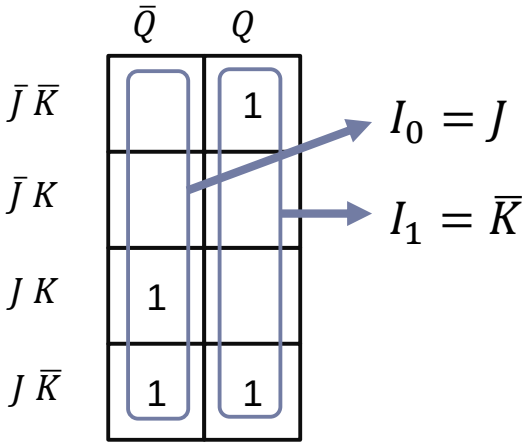
2. Binarna aplikacijska tabela pomnilne celice JK in vzbujevalna tabela za pomnilno celico D.

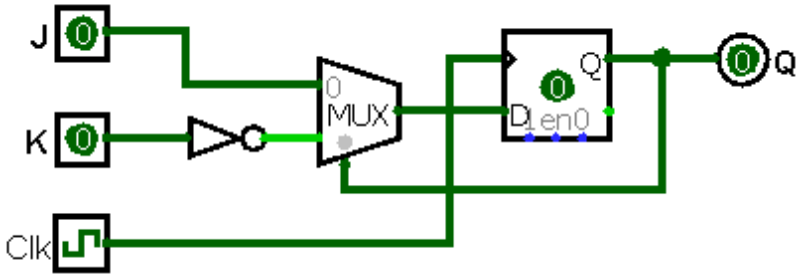
J	K	Q(t)	Q(t+1)	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

2. Izračun krmilnega vezja za pomnilno celico D

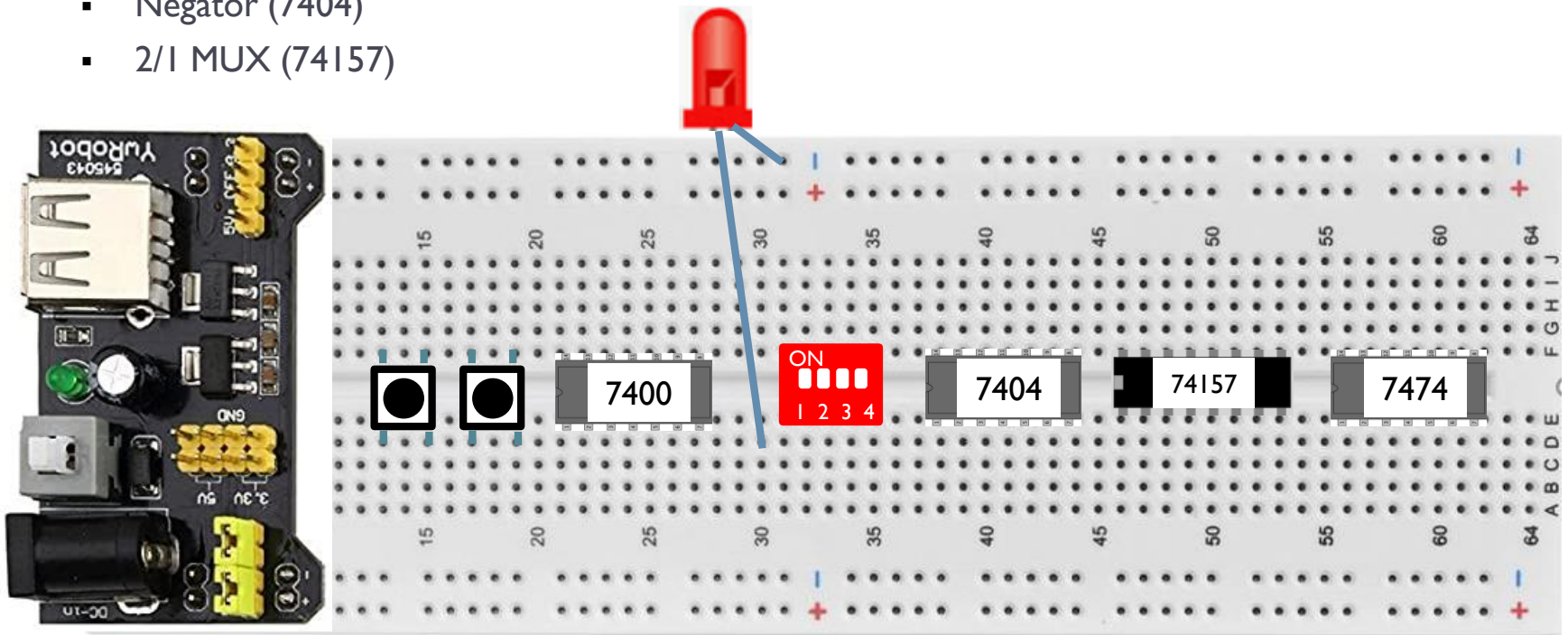
2/1 MUX

$(A_0 = Q)$



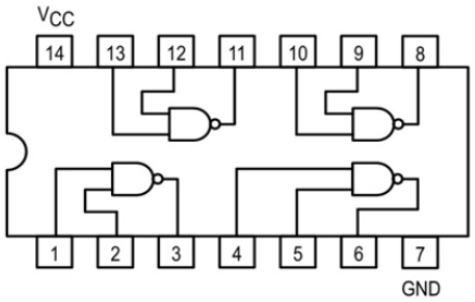


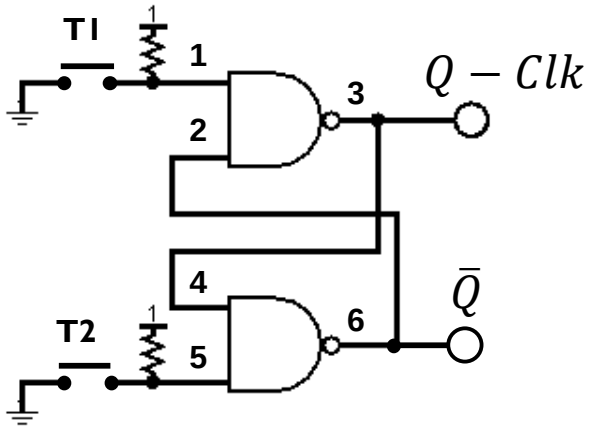
- Realizacija urinega signala in pomnilne celice JK
  - 2x Tipka
  - Stikala
  - NAND (7400)
  - Pomnilna celica D (7474)
  - Negator (7404)
  - 2/1 MUX (74157)

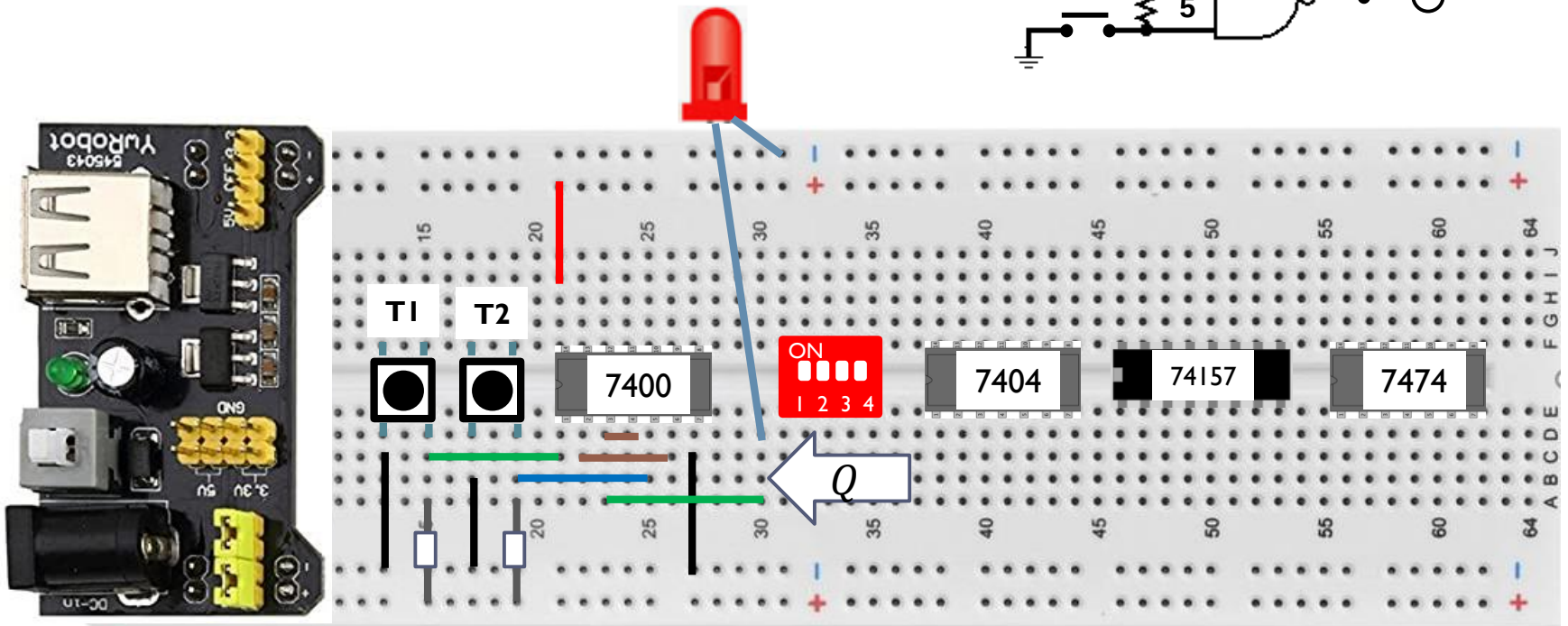


- Urin signal Clk:

  7400 - NAND

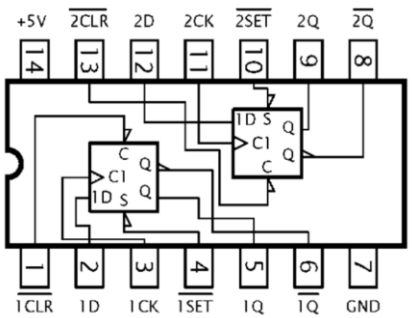


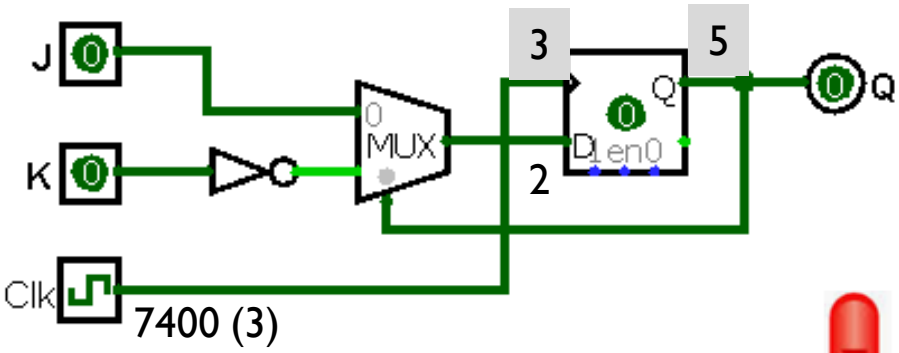


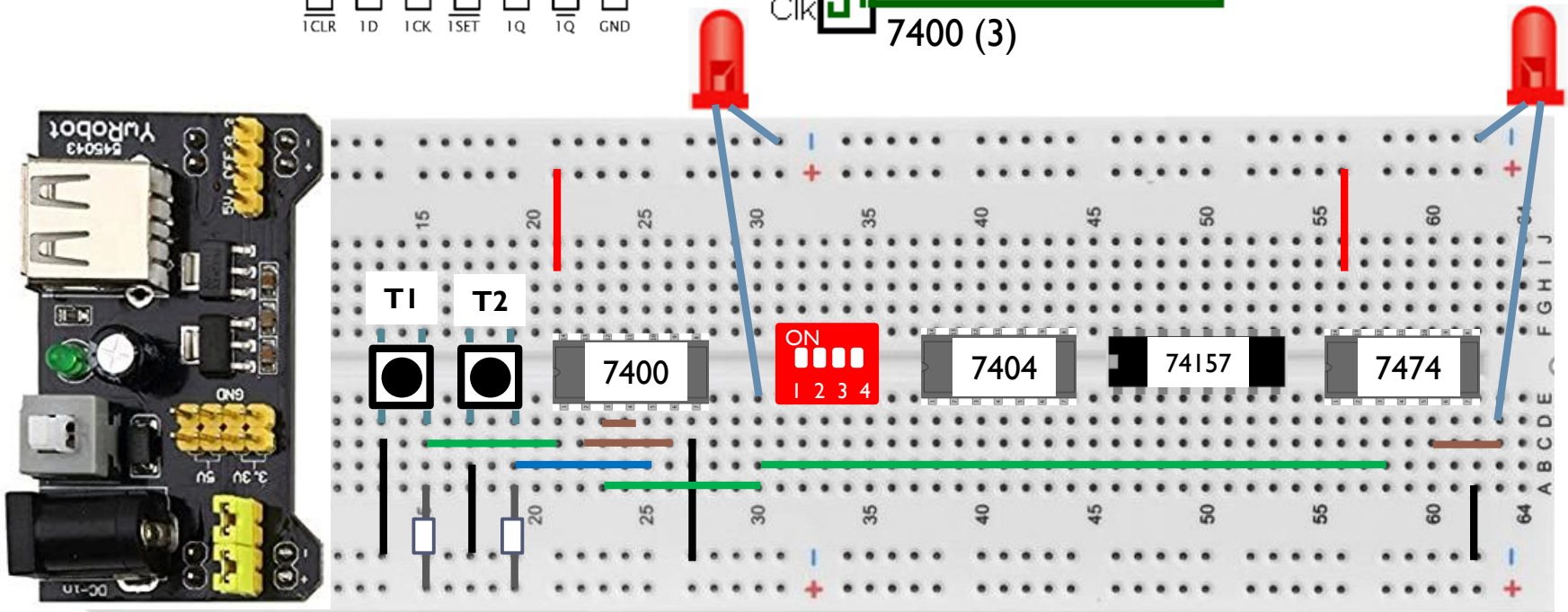


- Povezava JK pomnilne celice

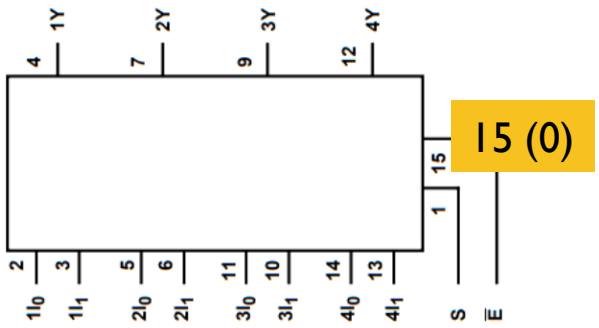
7474 - JK

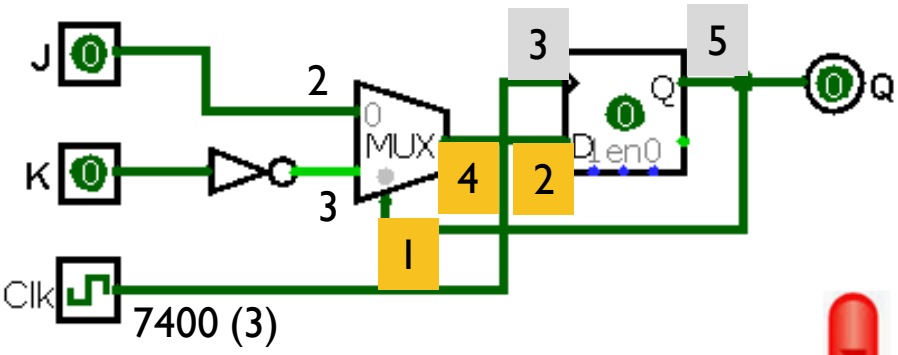


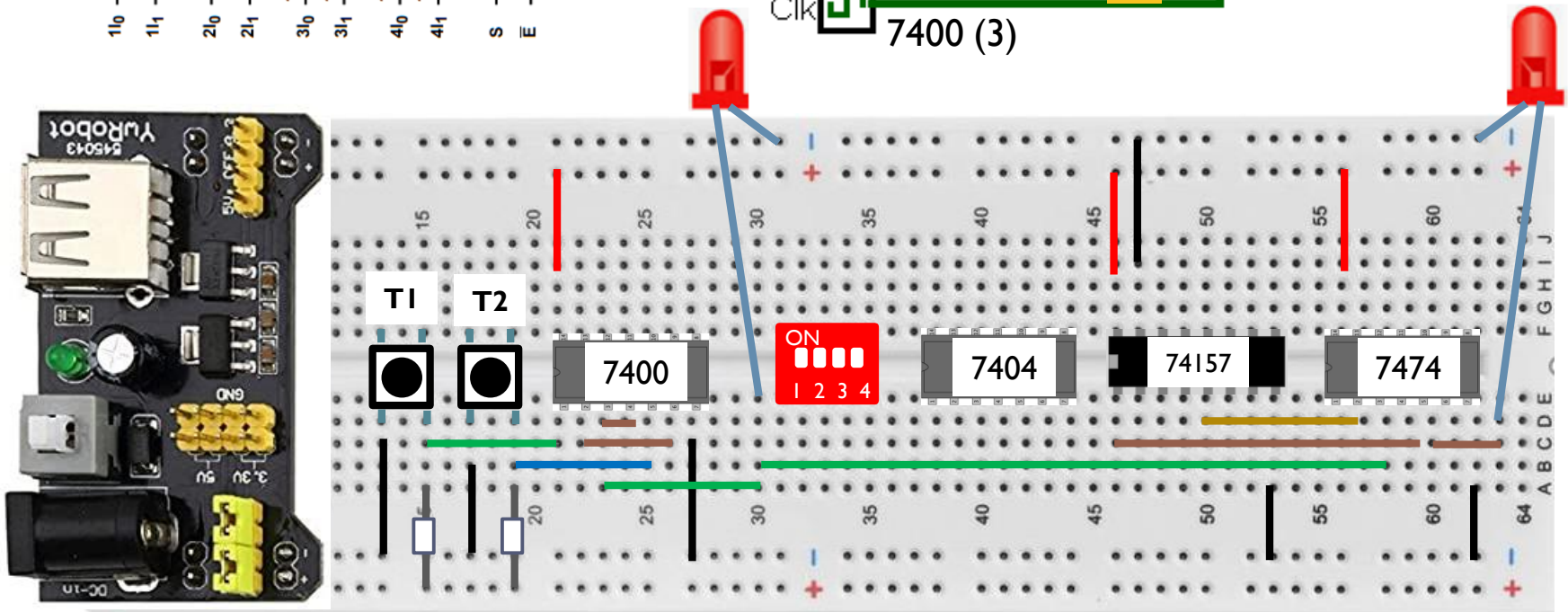




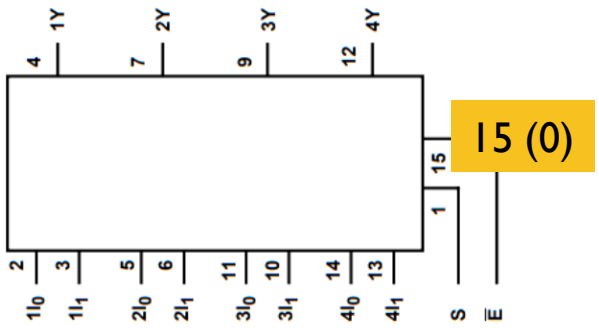
- Povezava 2/1 MUXa (74157) in pomnilne celice JK

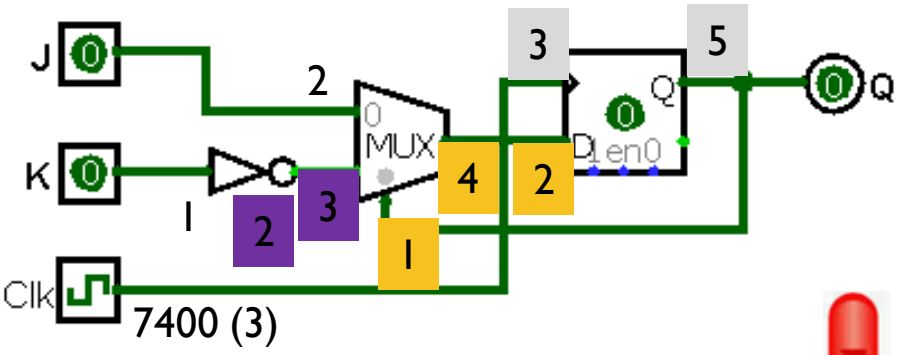


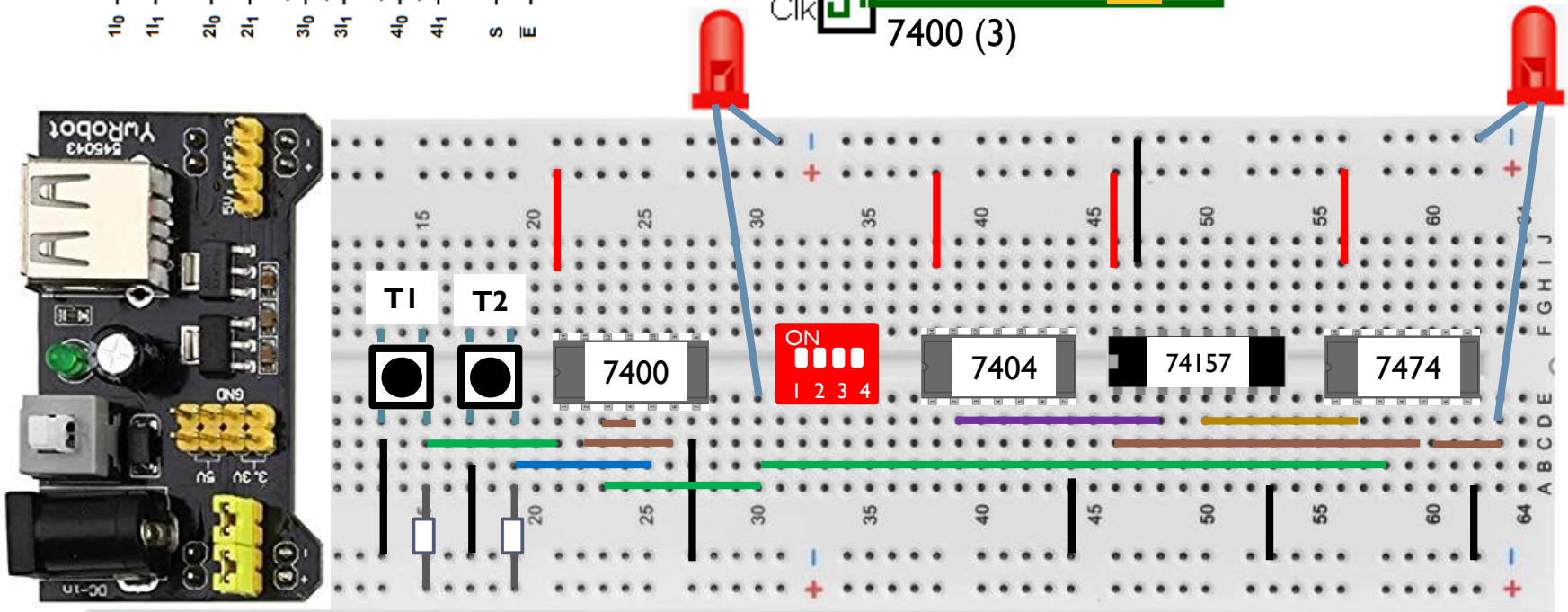




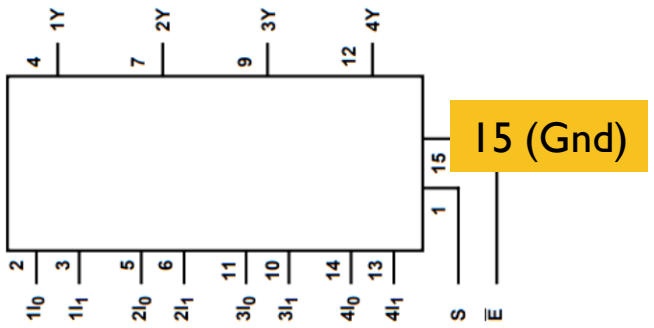
- Povezava 2/1 MUXa (74157) in vhodov J in K

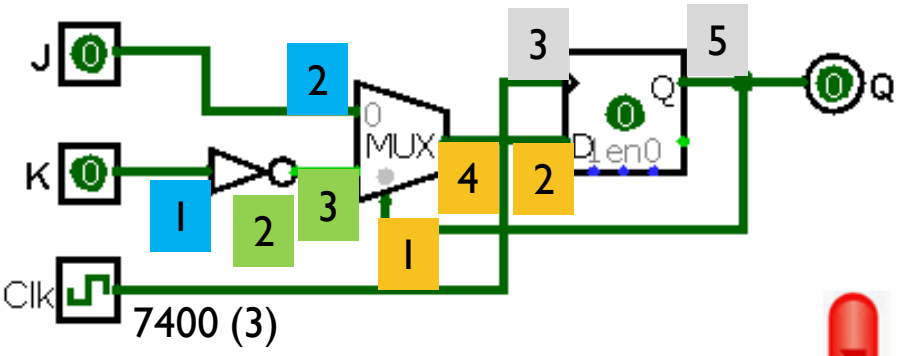


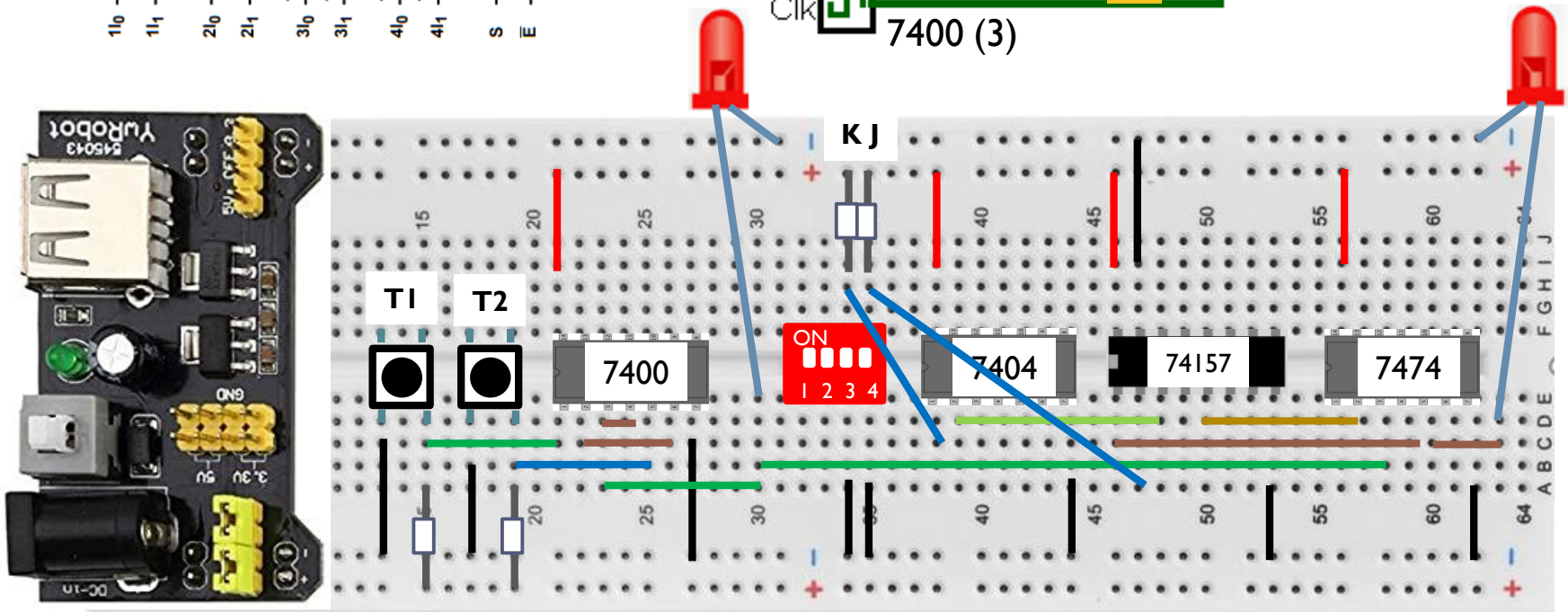




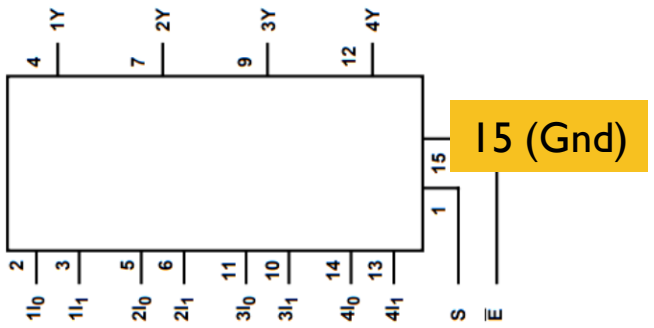
- Povezava 2/1 MUXa (74157) in stikal (vhoda J in K)

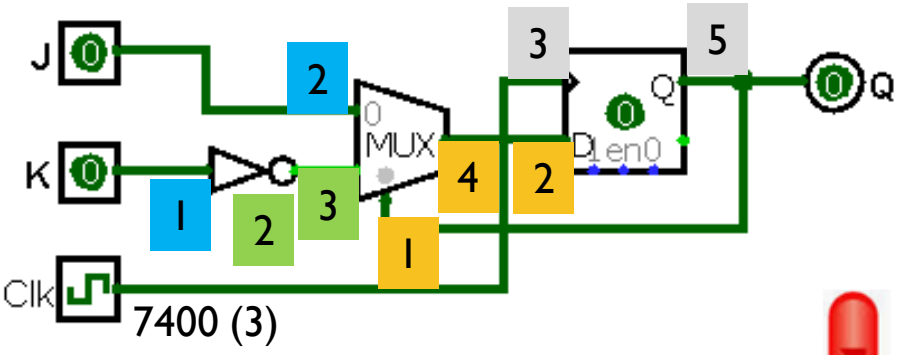


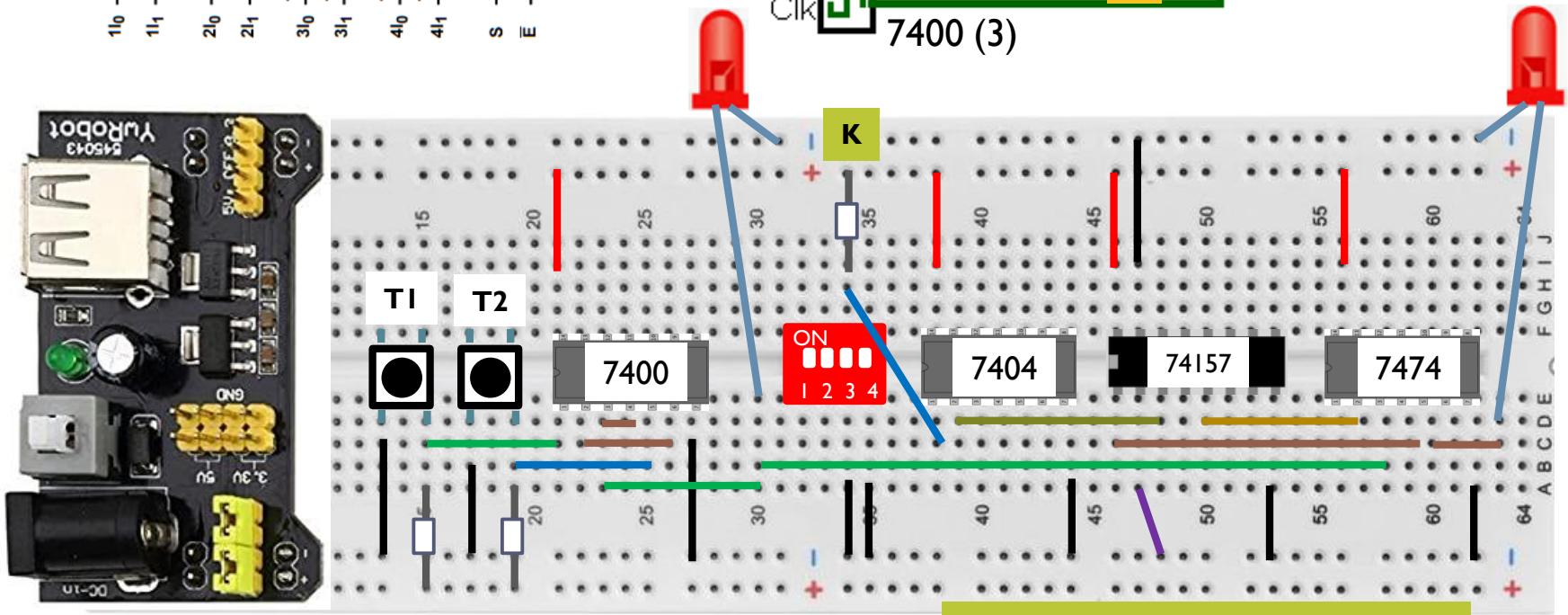




- Povezava 2/1 MUXa (74157) in stikal (vhoda J in K)- **nimamo upora**







J – izmenoma uporabimo Gnd in Vcc