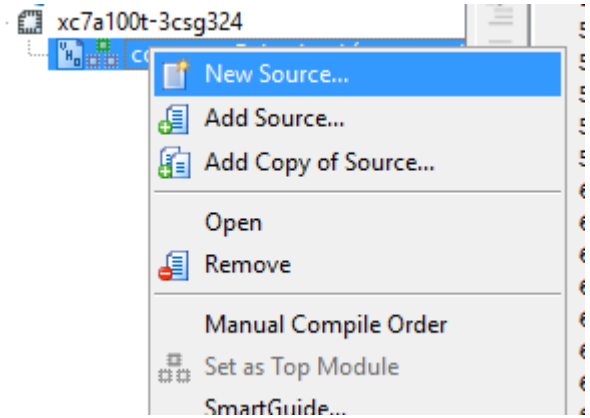
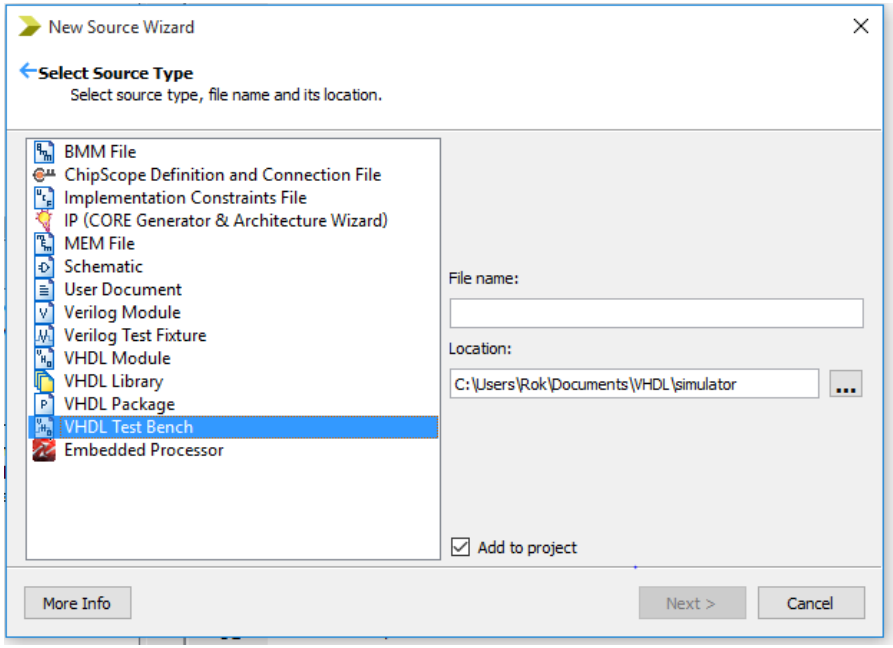
Digital Design

Simulator

- Add a new module to test another module





Simulator

- Select the module you want to test
- Generate a test-bench module that includes(connects) the chosen module
- Define the input signal values and changes to the input signals over time

Test bench

- Use a separate process to generate the clock

```
-- Instantiate the Unit Under Test (UUT)
uut: counter PORT MAP (
        clk => clk,
        rst => rst,
        count_out => count_out
      );

-- Clock process definitions
clk_process :process
begin
    clk <= '0';
    wait for clk_period/2;
    clk <= '1';
    wait for clk_period/2;
end process;
```

Test bench

- Define the other input in a separate process
  - Use assignement statements and wait instructions

```
wait for 100 ns;
wait for clk_period*10;
```

- clk_period is a defined constant

```
wait;
```

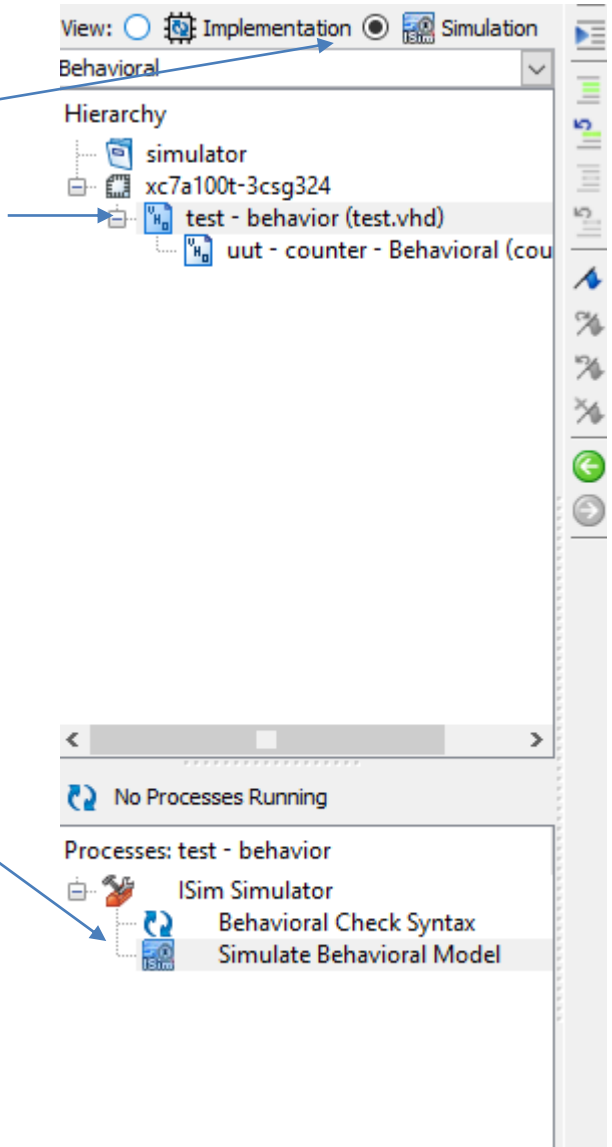
- wait for an undetermined amount of time

Test bench

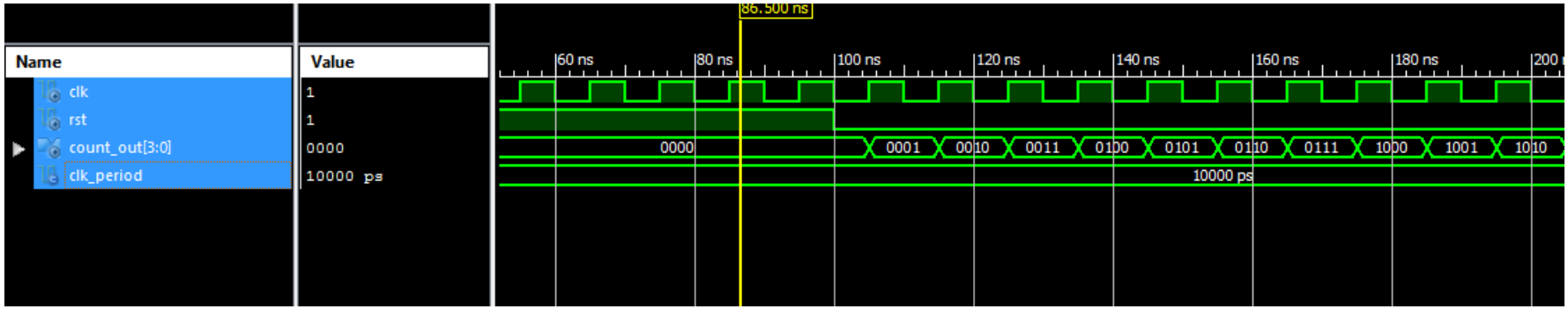
```
-- Stimulus process
stim_proc: process
begin
   rst <= '1';
   wait for 100 ns;
   -- hold reset state for 100 ns.
   rst <= '0';
   wait for clk_period*10;

   -- insert stimulus here

   wait;

end process;
```

Uporaba simulatorja

- Choose „simulation“
- Chose the module to test
- Run



Simulacija


86.500 ns
Name
Value
clk
rst
count_out[3:0]
clk_period
1
1
0000
10000 ps
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
180 ns
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
10000 ps